Smart Energy Efficient Gateway for Internet of Mobile Things

Igor Tcarenko[1], Yuxiang Huan[2], David Juhasz[3], Amir M. Rahmani[1], Zhuo Zou[2], Tomi Westerlund[1], Pasi Liljeberg[1], Lirong Zheng[2], and Hannu Tenhunen[1,2]
[1]Department of Information Technology, University of Turku, Turku, Finland
[2]Department of Industrial and Medical Electronics, KTH Royal Institute of Technology, Stockholm, Sweden
[3]Imsys AB, Stockholm, Sweden
Email: {igotca, amirah, tovewe, pakrli}@utu.fi, david.juhasz@imsystech.com, {yxhuan, zhuo, lirong, hannu}@kth.se

***Abstract*—Internet of Things (IoT) is a fast developing vision in which physical quantities are digitized, processed and analyzed. Internet of Mobile Things (IoMT) as one of new domains of IoT, due to mobility, requires a more demanding and rigorous solution in many aspects, especially in terms of energy efficiency. We propose a solution consisting of energy efficient and fast hardware platform for building IoMT Fog layer facilities. Experimental results are presented to prove superiority of the proposed hardware in several aspects to popular general purpose platforms.**

***Keywords*—Internet of Things, Internet of Mobile Things, Fog Computing, Smart Gateway, Energy Efficiency.**

I. Introduction

Actualization of IoT into the real world requires integration of several technologies. Cloud computing (i) is a critical constituent for expanding the ubiquitous computing systems infrastructure [1] and is crucial for realization of the complete IoT vision. Sensing nodes or edge nodes, which comprise sensor networks (ii) [2], constitute the "things" part of IoT. The mentioned components (i, ii) portray "Cloud" centric [3] and "Thing" centric [4] perspectives, the IoT can be seen from. Bonomi *et al.* [5] justified a need for a new important middle layer, called Fog (iii), to enhance mobility support, location awareness and low latency [6].

Most of the research focuses on systems with fixed sensor networks and fog layer facilities (FLF), that are bound to a specific location and have constant power supply. The stationary nature of such systems releases the problem of energy consumption which allows for unconstrained performance growth. Nonetheless there are systems, that have a demand for energy awareness at their core, which therefore cannot be neglected. Such systems carved a new sub-domain in IoT called Internet of Mobile Things (IoMT) [7], [8].

Leveraging general-purpose platforms' resources, FLF cover broad functional area, which varies from collecting data from the edge sensor nodes to complex data processing [9]. General-purpose nature of such platforms implies flexibility, which is often achieved at a cost of energy efficiency. In the systems, where energy efficiency is of a principal significance (IoMT, autonomous geo-distributed systems), this leads to decreased quality of service in general.

Energy efficiency of the entire solution is a cumulative result of efficiency of its parts. Therefore, hardware as a basement layer plays a vital role. Considering the mentioned downsides of the general purpose hardware we advocate the importance of the custom special dedicated hardware.

In this work, we propose a hardware platform which offers a feasible energy efficient yet fast solution for building FLF. Reconfigurable nature of the hardware offers high degree of flexibility which makes a platform a viable tool for adjusting energy consumption - performance trade-off. We compare the results of different algorithms in terms of execution time and energy consumption between the proposed platform and conventional general purpose platforms.

The rest of the paper is organised as follows: In Section II we describe the proposed hardware platform. The results are shown and discussed in Section III. In the last Section IV we conclude the paper, summarizing the work.

II. Hardware Platform Architecture

Existing popular embedded processors architectures such as MSP430 or ARM Cortex families are low-power, yet several drawbacks for emerging IoT applications limit the utility of the mentioned architectures. The drawbacks are inefficient logic utilization per cycle, high demands of memory spaces, and insufficient performance for data processing. Conventional application-specific instruction-set processors (ASIP) counterbalances energy efficiency and performance. However such processors are optimized for limited number of tasks and have little degree of reconfigurability, making it difficult to satisfy variety of needs of IoT applications. We present a reconfigurable and energy-efficient ASIP-based System-on-Chip(SoC) design, called Imsys IM3000-series controller, for IoT applications. The highlights of this design are:

(i) The microcoded cacheless ASIP architecture significantly reduces the silicon area and the power consumption. The unique micro-instructions are designed to maximize the utilization of the logic per cycle and avoid "dark silicon".
(ii) Reconfigurability feature is achieved by means of reprogrammable microcoding in RAM memory. The processor is able to reload different constitutions of instruction-sets according to different applications. It optimizes hardware

978-1-5090-6196-9/17/$31.00 ©2017 IEEE

resources and logic operations for specific tasks, and also reduces the demands of data movements.

(iii) Java Virtual Machine bytecodes have been microcoded and thus included in its native instruction set, resulting in more efficient Java code execution.

(iv) The SoC integrates AD/DAs, Ethernet MAC, and timing systems, making it well-suited for Internet-of-Things applications.

The implementation and evaluation results indicate that the proposed architecture is superior to ARM Cortex-M3 and ARM9 architectures in terms of performance (execution time) for C and Java as general purpose MCU. It exhibits $>4\times$ code density and $>1.5\times$ energy-efficiency compared to similar technologies. In addition, the optimized microcode provides $10\times$ speedup for application-specific tasks such as Fast Fourier Transform and data encryption.

High computational performance is guaranteed by efficient utilization of the 8-bit ALU, memories and other hardware units managed by unique microinstructions. In addition, an 8-bit multiply accumulate unit incorporates a 24-bit shifter, which empowers DSP operations. All the hardware units and data paths are directly organized and controlled by the 80-bit micro-instructions. In contrast to RISC architecture, which relies on extending data-path width for speed, our approach exploits advanced multi-cycle instructions to increase the hardware utilization and energy efficiency, while keeping the performance at a high level. The fixed general-purpose micro-programs are pre-programmed into an 80 KB ROM in order to save area and energy. A 40 KB RAM is designed for reprogramming the micro-instructions to facilitate reconfigurability for different sets of application-specific instructions.

Exploiting micro-instructions allows for decreased area footprint (25% compared to MSP430 and 20% compared to ARM Cortex-M3). High code densities relaxes the access frequency to the external memory and thus lower the power consumption. Moreover, the microcode architecture allows for cache free design - this reduces power utilization.

Fabricated with a 180 nm standard CMOS process, the silicon area of the entire SoC is 9.94 mm^2 with a processor core area of 1 mm^2 . The maximum current consumption for the SoC, operating at 167 MHz, is 32.5 mA

III. Results

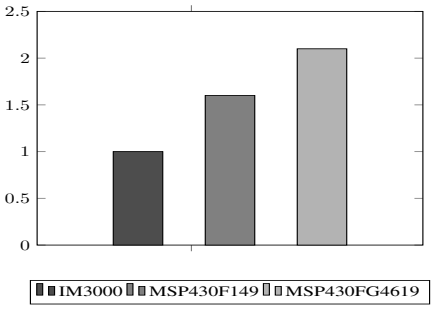
The prototype was evaluated using standard benchmark programs and compared to other SoCs of the similar process.

The tests show, that the energy efficiency is superior to MSP430 and ARM Cortex M3 for all the benchmarks (Table 1a, Fig. 1b). The cacheless ASIP outperforms Cortex-M3 performance-wise approximately twice on float data processing, although the data path is only 8 bits.

Enabling computationally intensive tasks at lower energy cost will unlock the new range of tasks for the devices, which nowadays are considered to be resource constrained. This will shift the focus from the Cloud, as the main analytical and decision-making center, to the Edge of the network, thus promoting the emergence of independent, highly autonomous ubiquitous computing systems systems.

	EMB	FIR	Dhrystone	Whetstone
IM3000	0.74	70	225	90
MSP430-F149	0.71	180	290	169
MSP430-FG4619	1	247	262	236

(a) Energy consumptions for different benchmark applications.



(b) Normalized energy consumption.

Fig. 1: Energy consumption experimental results for this work, MSP430F149 and MSP430FG4619.

References

[1] Ramon Caceres and Adrian Friday. Ubicomp systems at 20: Progress, opportunities, and challenges. *IEEE Pervasive Computing*, (1):14–21, 2011.

[2] Luigi Atzori, Antonio Iera, and Giacomo Morabito. The internet of things: A survey. *Computer networks*, 54(15):2787–2805, 2010.

[3] Jayavardhana Gubbi, Rajkumar Buyya, Slaven Marusic, and Marimuthu Palaniswami. Internet of things (iot): A vision, architectural elements, and future directions. *Future Generation Computer Systems*, 29(7):1645–1660, 2013.

[4] Tomás Sánchez López, Damith C Ranasinghe, Mark Harrison, and Duncan McFarlane. Adding sense to the internet of things. *Personal and Ubiquitous Computing*, 16(3):291–308, 2012.

[5] Flavio Bonomi, Rodolfo Milito, Jiang Zhu, and Sateesh Addepalli. Fog computing and its role in the internet of things. In *Proceedings of the first edition of the MCC workshop on Mobile cloud computing*, pages 13–16. ACM, 2012.

[6] Flavio Bonomi, Rodolfo Milito, Preethi Natarajan, and Jiang Zhu. Fog computing: A platform for internet of things and analytics. In *Big Data and Internet of Things: A Roadmap for Smart Environments*, pages 169–186. Springer, 2014.

[7] Nanjangud Narendra and Prasant Misra. Research challenges in the internet of mobile things. *Newsletter*, 2016.

[8] Klara Nahrstedt. Internet of mobile things: challenges and opportunities. In *PACT*, pages 1–2, 2014.

[9] Tuan Nguyen Gia, Mingzhe Jiang, Amir-Mohammad Rahmani, Tomi Westerlund, Kunal Mankodiya, Pasi Liljeberg, and Hannu Tenhunen. Fog computing in body sensor networks: An energy efficient approach.