Low-Power and Widely Tunable Linearized Biquadratic Low-Pass Transconductor-C Filter

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***Abstract*—A sixth-order low-pass transconductor-C filter with a very wide tuning range ($f_c = 100$ Hz to 10 MHz) is presented. The wide tuning range has been achieved without using switchable components or programmable building blocks. A single-stage folded cascode transconductor is employed to implement the proposed filter. A modified biquadratic topology is introduced to improve linearity performance of the filter over its tuning range. Power consumption of the filter scales linearly with cutoff frequency (60 pW/Hz/pole). Implemented in 0.18-μm complementary metal–oxide–semiconductor technology, the filter exhibits relatively constant noise and linearity performance over its entire tuning range and occupies a silicon area of 0.16 mm^2 (0.027 mm^2/pole).**

***Index Terms*—Biquadratic filter, complementary metal–oxide–semiconductor (CMOS) integrated circuits, continuous-time filters, g_m-C filter, subthreshold, transconductor-C, weak inversion, widely tunable.**

I. Introduction

EMERGING new markets for multipurpose and multistandard applications, such as in software-defined radios and biomedical implantable systems, have made the design of reconfigurable integrated circuits very desirable [1]–[3]. In this brief, the main goal is to implement a widely tunable cutoff frequency transconductor-C (g_m-C) filter with scalable power dissipation. This continuous-time filter will be a part of a mixed signal system in which power dissipation of the entire system can be adjusted with respect to operating frequency using a central power management unit [4]. To obtain a power-efficient and widely tunable filter, it is very desirable to have the circuit power consumption P_{diss} proportional to the cutoff frequency of filter (f_C), i.e., $P_{\text{diss}} \propto f_C$.

Designing continuous-time filters with a wide tuning range with an acceptable linearity and dynamic range (DR) performance turns out to be very challenging. Some circuit techniques for extending the tuning range by changing the biasing condition of devices, particularly metal–oxide–semiconductor (MOS) devices biased in a triode region, have been reported [2]. Using bipolar devices or MOS transistors biased in a subthreshold regime that exhibit exponential I–V characteristics can help to extend the frequency tuning range, such as in log-domain filters [5]. The other solution for extending the operating frequency range is using switchable or programmable components and building blocks [6]–[9], which requires a very careful design to minimize the extra silicon area required for programmable components.

In this brief, a linearized biquadratic g_m-C filter that uses simple differential folded cascode operational transconductor amplifiers (OTAs) is presented, based on a topology introduced by Tajalli and Leblebici [10]. In this approach, a modified biquadratic topology has been used, which relaxes requirements on transconductor linearity. Unlike the other techniques, which are used for improving filter linearity performance (such as linearized transconductors [9] and reduction of a voltage swing at inputs of transconductors [11]), the proposed approach does not degrade the DR or the tuning range of the filter. Therefore, this topology is very suitable for implementing widely tunable continuous-time filters without employing switchable or programmable components.

II. Widely Tunable g_m-C Filter

The g_m-C topology is very suitable for implementing very high [8] or very low frequency filters [12], [13]. The main problem associated with this type of filters is poor linearity performance of transconductors, which are the main building blocks for implementing g_m-C filters. A transconductor should remain linear for an entire input differential voltage swing, which is generally very difficult to achieve. Many complex circuit topologies are proposed to enhance linearity performance, which on the other hand degrade frequency and noise performance of a filter. This problem becomes more evident in widely adjustable filters, where transconductance needs to be varied over a very wide range.

In the following, a new approach for improving linearity of biquadratic g_m-C filters will be introduced. Using this technique, simple transconductor topologies can be employed, which helps to keep the area small.

A. Proposed Biquadratic Filter Topology

A single-stage differential pair OTA, as illustrated in Fig. 1(a), is one of the simplest topologies that can be used for implementing g_m-C filters. Transconductance of this OTA can also be tuned over a very wide range, whereas input differential pair devices can be biased in weak, moderate, and strong inversion regimes. However, the main drawback of this topology is its limited linearity range. Indeed, the input voltage swing of this OTA is limited to a fraction of U_T in weak inversion (independent to bias current) and a fraction of $V_{DS,\,\text{sat}}$ (proportional

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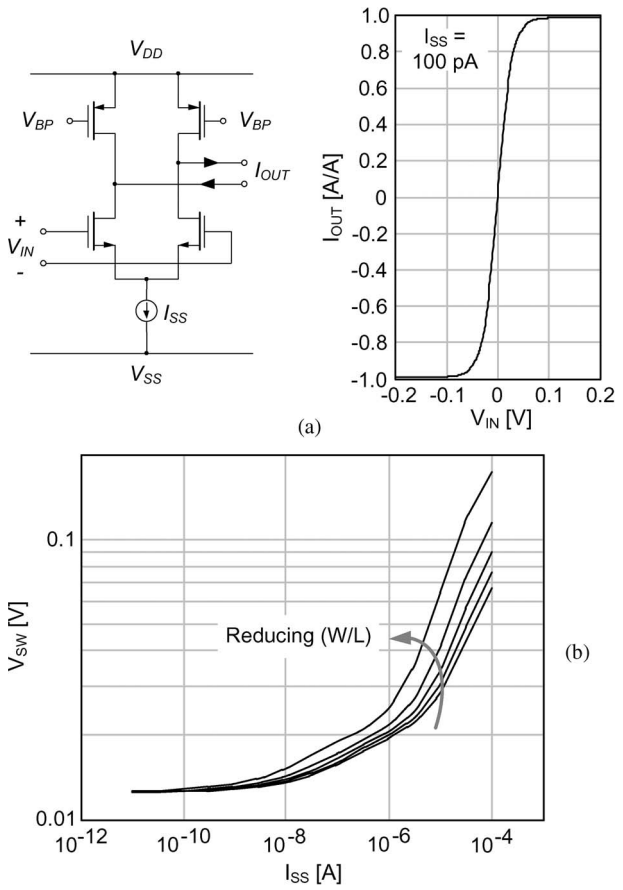

Fig. 1. (a) Single-stage differential OTA can be used as a widely adjustable transconductor. Typical I–V characteristics of the differential pair OTA is also shown. (b) Maximum voltage swing at the input of the differential pair OTA to keep the nonlinearity of output current below 5%.

to $\sqrt{I_{\rm SS}}$) in strong inversion, which is not sufficient for most of the applications [14], [15]. Fig. 1(b) depicts the maximum input voltage swing to have a nonlinearity value of less than 5% at the output current of the transconductor shown in Fig. 1(a). In the figure, it can be seen that the maximum acceptable voltage swing is almost constant and less than 20 mV as long as the devices are in a subthreshold regime. However, by increasing bias current and entering into strong inversion, this range increases. To compensate the poor linearity performance of this transconductor, a modified biquadratic topology is proposed in Fig. 2.

Fig. 2(a) shows a conventional second-order biquadratic g_m-C filter. In this simplified circuit diagram, there are two transconductors that convert voltage to current as follows:

$$I_M = G_{m1} \cdot [(V_{\rm IP} - V_{\rm IN}) - (V_{\rm OP} - V_{\rm ON})] \quad (1)$$
$$I_O = G_{m2} \cdot [(V_{\rm MP} - V_{\rm MN}) - (V_{\rm OP} - V_{\rm ON})] \quad (2)$$

where $G_m = G_{m1} = G_{m2}$, and I_M and I_O are denoting the differential currents that flow into capacitors C_M and C_O, correspondingly. The frequency response of the filter is as follows:

$$H(s) = \frac{\omega_0^2}{s^2 + (\omega_0/Q)s + \omega_0^2} \quad (3)$$

where $\omega_0 = G_m/\sqrt{C_M C_O}$ and $Q = \sqrt{C_O/C_M}$. Based on (1) and (2), each transconductor converts two differential voltages

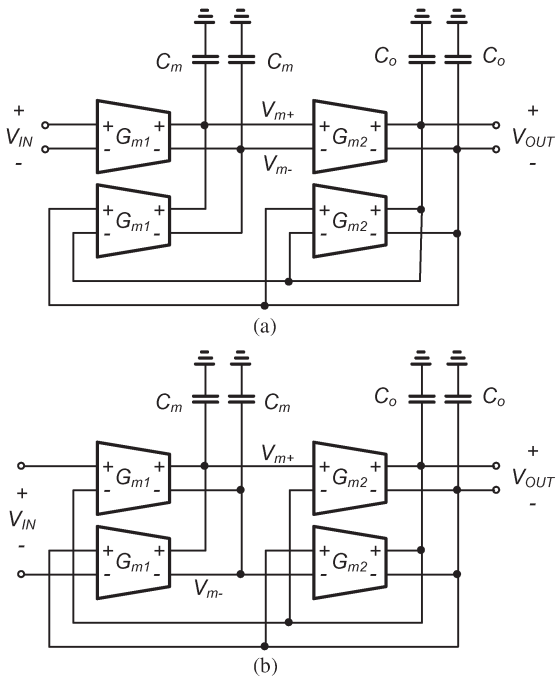

Fig. 2. Biquadratic g_m-C filter. (a) Conventional topology. (b) Modified topology with improved linearity performance.

to a current, and then, the output currents are summed together. In the configuration shown in Fig. 2(a), a linearity problem arises when the transconductors need to convert high swing differential voltages (such as $V_{\rm IP} - V_{\rm IN}$) to current. In this case, the transconductor needs to be very linear for the entire input voltage swing to have a low distortion output current, which is proportional to $G_m(V_{\rm IP} - V_{\rm IN})$. To alleviate this requirement, (1) and (2) can be rewritten as follows:

$$I_M = G_{m1} \cdot [(V_{\rm IP} - V_{\rm OP}) + (V_{\rm ON} - V_{\rm IN})] \quad (4)$$
$$I_O = G_{m2} \cdot [(V_{\rm MP} - V_{\rm OP}) + (V_{\rm ON} - V_{\rm MN})]. \quad (5)$$

In this manner, the total current delivered to each capacitance and, hence, the filter transfer function presented in (3), remain unchanged. However, each transconductor needs to convert the difference of the two signals that are in phase (or have a phase difference smaller than 90° for in-band frequencies), resulting in a much smaller input voltage swing. Therefore, it can be expected that the linearity performance of the filter improves considerably. Fig. 2(b) illustrates the implementation of the proposed biquadratic filter based on (4) and (5) [10].

Fig. 3 compares the linearity performance of the two filters shown in Fig. 2 based on behavioral modeling. Here, it is assumed that the input devices are biased in the subthreshold regime, and frequency is normalized to the cutoff frequency of the filter. For very low input frequencies, the phase differences between V_I and V_O and also between V_M and V_O are very small. Hence, linearity improvement is considerable, and the filter exhibits less harmonic distortion in higher input voltage amplitudes $A_{\rm IN}$. By increasing the frequency and, hence, increasing the phase difference between the input signals, linearity enhancement degrades; however, it is still much better for the modified topology. For very high frequencies, linearity performance of the two configurations becomes comparable.

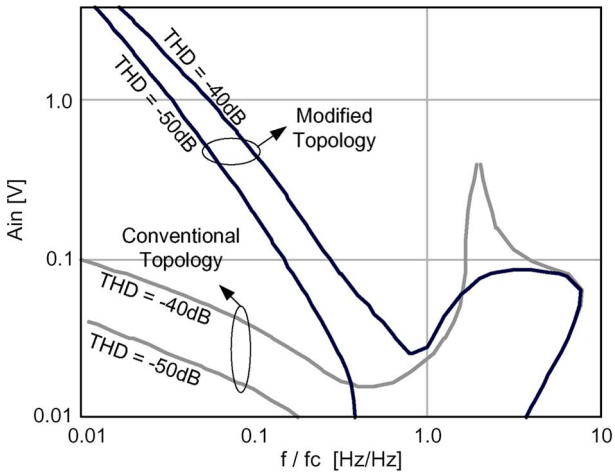

Fig. 3. Comparing the linearity performance of the two biquadratic filters shown in Fig. 2 based on behavioral modeling. Here, it is assumed that the input differential pair transistors are biased in the subthreshold regime, and transconductance can be calculated based on (6) without including secondary effects such as mobility degradation or high-field effects. In this figure, $A_{\rm IN}$ represents the peak voltage amplitude of the input signal.

B. Observations

As it can be deduced from (1)–(5), the linearity of both the conventional and modified topologies depends on two factors: the voltage swing at the input of each transconductor and the linearity performance of the transconductors. With the same transconductor circuits, the topology in Fig. 2(b) exhibits better linearity if the voltage swing at the input of each transconductor is less than the voltage swing at the input of the counterpart transconductors in Fig. 2(a). As far as this condition is satisfied, this observation remains valid and does not depend on filter topology, the order of the filter, circuit implementation of the transconductors, and fabrication technology.

The maximum linearity improvement expected from the modified topology can be achieved when the two input signals of the transconductors (such as V_I and V_O) are in phase and with the same amplitude. Therefore, in cases where the transconductors need to deal with in-phase signals but different magnitude values or with the same amplitude but different phases, such as in some all-pass or bandpass configurations, efficiency of this technique will decline.

Similar improvement can be achieved for the devices in strong inversion. Therefore, this technique improves the linearity performance of the filter regardless of the operation region of the devices. Hence, this circuit can be used for implementing widely tunable g_m-C filters with good linearity performance when the devices are biased in weak, moderate, and strong inversion regions. It is possible to improve the linearity performance of the filter even further using other linearizing techniques, such as using source degeneration resistance [16].

It should be mentioned that this technique is applicable to other types of g_m-C filters as well, such as gyrator-based topologies. The main issue associated with this technique is degradation of the common-mode rejection ratio similar to other pseudo-differential-based topologies. Therefore, if necessary, special circuit and layout techniques are necessary to be applied for reducing the effect of common-mode signals.

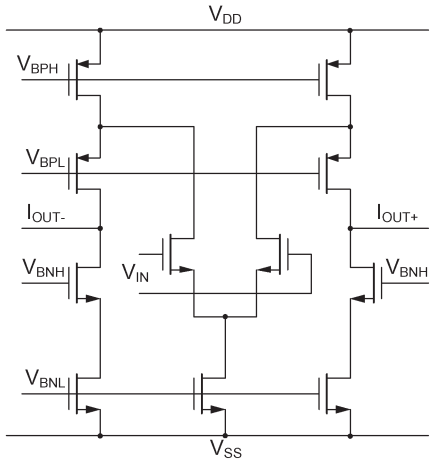

Fig. 4. Schematic of the folded cascode transconductor used to implement the widely tunable filter.

C. Dynamic Range (DR)

As long as the input differential pair transistors of the proposed OTA are in a subthreshold regime, large-signal transconductance can be expressed by

$$G_m = \frac{\partial I_{\rm OUT}}{\partial V_{\rm IN}} = \frac{I_{\rm SS}}{2nU_T} \cdot \frac{1}{\cosh^2\left(V_{\rm IN}/(2n_nU_T)\right)}. \quad (6)$$

In this case, the linearity performance of the transconductors does not depend on the bias current of the OTA, $I_{\rm SS}$, and it is expected that the filter exhibits constant linearity performance. By entering the strong inversion region for large current values, however, linearity starts to improve. On the other hand, it is expected that the total output root mean square noise remains independent of the cutoff frequency of the filter. Assuming that $G_{m1} = G_{m2} = G_m$ in Fig. 2, it can be concluded that the output noise power density $v^2_{n,\,\rm OUT}$ will be

$$v^2_{n,\,\rm OUT} = |H(j\omega)|^2 \cdot \left(1 + \frac{\omega^2}{\omega_0^2 Q^2}\right) \cdot \frac{i^2_{n,\,G_m}}{G_m^2} \quad (7)$$

where, $i^2_{n,\,G_m} = 4kT\gamma_{G_m} \cdot G_m$ is the current noise corresponding to each transconductor (γ_{G_m} is the noise excess factor for the proposed transconductor), and $H(j\omega) = H(s)\,|_{s=j\omega}$ is calculated in (3). Therefore, the output noise power density is inversely proportional to G_m. On the other hand, since filter bandwidth is proportional to G_m, the total output noise power will remain unchanged with scaling the bias current $I_{\rm SS}$ or equivalently G_m. This means that the signal-to-noise ratio (SNR) of the filter remains constant as long as the differential pair devices in the OTA are in subthreshold. By moving toward strong inversion, the SNR will improve proportional to linearity improvement.

In these calculations, only thermal noise has been considered. For a more precise calculation, particularly in low operating frequency range, it is necessary to include the effect of flicker noise as well. As the voltage magnitude of the flicker noise does not depend on the bias current or the transconductance of the devices, the total noise of the filter due to flicker noise will not remain unchanged when the cutoff frequency of the filter changes. In this brief, the size of transistors have been selected to be large enough to minimize the effect of flicker noise.

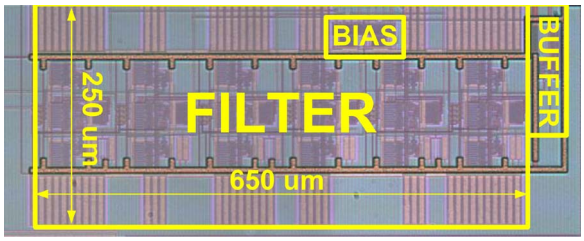

Fig. 5. Chip photomicrograph of the filters implemented in conventional 0.18-μm CMOS technology.

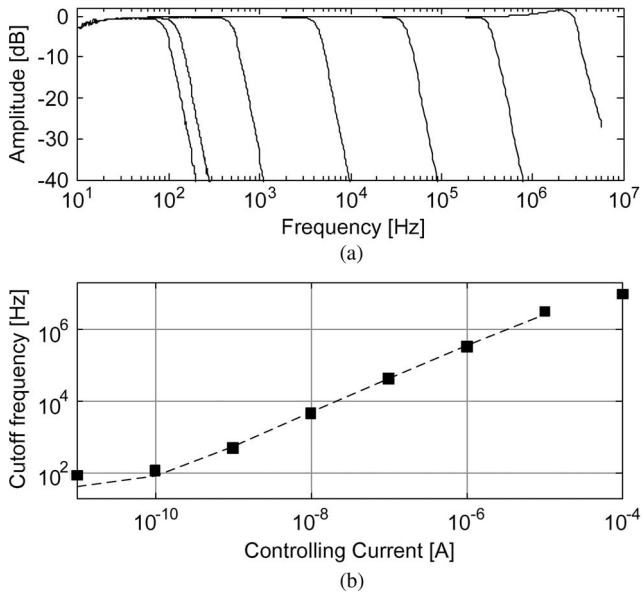

Fig. 6. Measured g_m-C filter characteristics. (a) Frequency transfer characteristics. (b) Cutoff frequency versus tuning current.

III. Design Example

A simple OTA with a folded cascode topology has been used to implement two sixth-order Butterworth g_m-C filters based on Fig. 2(a) and (b). Folded cascode OTAs (see Fig. 4) consume more power compared with simple differential pair OTAs; however, they can provide a wider input common-mode range, which can improve linearity performance in both topologies shown in Fig. 2. To reduce chip area, a single filter, which is switchable between the two topologies, has been designed. For this purpose, each biquadratic stage uses two complementary MOS (CMOS) transmission gate switches to deliver the input signals to the transconductors according to Fig. 2(a) or (b). In this design, MOS capacitors have been used to further reduce the required silicon area.

Simulations show that both filters exhibit similar frequency responses and input-referred noise values for the entire tuning range. The achievable cutoff frequency tuning range is $f_c = 50$ Hz to 2 MHz for a bias current of $I_{\rm SS} = 10$ pA to 10 μA.

IV. Experimental Results

The proposed filters based on the topologies shown in Fig. 2 have been implemented in 0.18-μm CMOS technology. A chip photomicrograph of the proposed sixth-order filters is shown in Fig. 5. The entire circuit occupies a silicon area of 650 $\times$ 250 μm^2 (micro-meter square). To examine the efficiency of the proposed approach, no technique for linearizing the transconductors at the transistor level has been used.

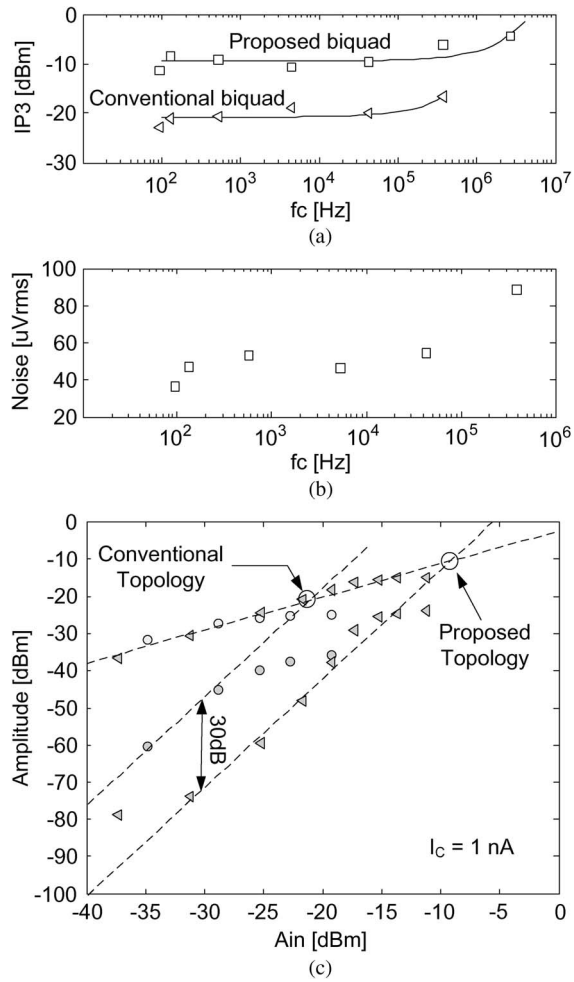

Fig. 7. Measured results. (a) IP3 and (b) noise power at different cutoff frequencies. As the measured noise level of both two designs is the same, only one has been shown. (c) HD3 of the proposed g_m-C filter in comparison with the conventional topology when $I_C = 1$ nA.

The measured frequency response of the filter versus the input controlling current I_C is shown in Fig. 6(a). In this design, the controlling current is set to be equal to the tail bias current of the transconductors, i.e., $I_C = I_{\rm SS}$. As can be seen in this figure, the controlling current can be as low as $I_C = 10$ pA for $f_C \simeq 80$ Hz. Average normalized power consumption of the proposed sixth-order filter is 344 pW/Hz. Fig. 6(b) shows the tuning range of this filter in comparison to the simulation results for $I_C = 10$ pA to 100 μA. As the cutoff frequency approaches to its upper limit, the quality factor of the filter changes mainly due to the effect of parasitic poles of the transconductors. Conventional techniques for adjusting the quality factor can be employed to alleviate this problem.

The measured third-order intermodulation intercept point (IP3) and the total noise power of these two topologies are shown in Fig. 7(a) and (b). As expected, the noise level remains relatively constant for the entire tuning range, and measurements show that the total noise power is the same for both topologies. As stated in Section II-C, the noise power due to flicker noise does not remain constant with changing cutoff frequency. Careful transistor sizing has been done to minimize the

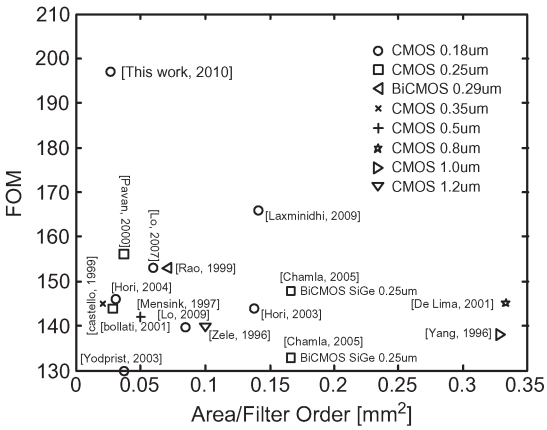

Fig. 8. FOM comparison to some other reports versus normalized filter area (area is normalized to the order of the filter) based on [7]–[9] and [17]–[26].

effect of flicker noise. As long as the input differential pair devices are in a subthreshold regime, the filter exhibits a constant IP3. When the controlling current increases, the devices enter strong inversion, and IP3 improves. Compared with the conventional topology, the IP3 of the proposed filter is improved by 10 dB. Meanwhile, measurement results show that the in-band harmonic distortion of the modified biquadratic filter is 25 to 35 dB smaller. Fig. 7(c) shows the measured third harmonic distortion (HD3) results for these two topologies for $I_C = 1$ nA.

Fig. 8 compares the figure of merit (FOM) of this brief with some previously published designs based on a definition introduced in [17]

$$\text{FOM} = 10\log\left(\frac{IMFDR_{\text{lin.}} \times \Gamma_f}{P_{\text{diss}}/(N \times f_c)}\right) \tag{8}$$

in which $IMFDR_{lin.}$ stands for intermodulation-free DR (without unit), N represents the order of filter, and Γ_f indicates the ratio of the maximum to minimum filter cutoff frequencies. Fig. 8 shows that the proposed filter exhibits a much better FOM compared with other already published designs. This improvement is mainly due to the simple topology used to implement the circuits, which has also resulted in a very area- and power-efficient implementation, as illustrated in Fig. 8.

V. Conclusion

In this brief, we have introduced a continuous-time g_m-C filter with a very wide tuning range. The proposed filter uses transconductors with differential input pairs and a folded cascode output stage in a balanced configuration. The simple structure of the transconductor makes it possible to change transconductance of the cells in a very wide range. Measurements show that linearity remains almost constant for the entire tuning range. Power consumption scales proportionally to cutoff frequency, which makes this topology very power efficient. Implemented in 0.18-μm CMOS technology, the area of the filter is 0.16 mm^2 and consumes 60 pW/Hz/pole.

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