Digital Control of an Interleaved BCM Boost PFC Converter with Fast Transient Response at Low Input Voltage

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***Abstract*—This paper presents the design of a digital controller for a 600 W Boundary-Conduction-Mode (BCM) interleaved boost converter used in an ac-dc Power-Factor-Correction (PFC) power supply. The output voltage of a typical boost PFC rectifier contains a 2^{nd} harmonic ripple. Therefore to achieve good power factor, the output voltage compensator must have a low bandwidth, in order to sufficiently attenuate this 2^{nd} harmonic component. As a result, the output voltage can suffer from poor transient response, especially at low input voltage. In this paper, a small-signal model of the output voltage dynamics is derived, where it is shown the open-loop gain of the system decreases with low input voltage. As a result, the output voltage transient response also deteriorates at low levels of input voltage. This can lead to poor voltage transient response for boost PFC converters that are designed to have an operating input line voltage range from 85 to 265 V. Having poor output voltage transient response is undesirable as it can lead to high peak over shoot on the output capacitors, or even worse, lead to an output voltage tracking failure. To correct this behaviour, an adaptive digital voltage compensator is designed to change gain at low input voltage, to ensure the output voltage maintains good transient response. Finally, the derived small-signal analysis, and output voltage compensator performance are experimentally verified on a 600 W interleaved BCM converter.**

I. Introduction

Power-Factor Correction (PFC) is a widely used solution to limit the input current harmonics of ac-dc power supplies in order to meet strict regulations. The most popular choice of circuit to implement PFC has been the combination of an input rectifier and boost circuit. For lower-power applications ($<$ 300 W), operating the boost converter in BCM is the preferred choice, due to advantages such as reduced inductor size and reduced switching losses via soft-switching. Interleaving two phases of a BCM boost converter brings additional advantages, such as input current ripple cancellation and reduced output capacitor current ripple, allowing the Boundary-Conduction-Mode (BCM) topology to be used at power levels in the region 300 - 600 W [1], [2]. At higher power levels, the high rms switch current and high differential mode conducted emissions degrade the use of the BCM topology, making the boost converter in CCM (Continuous Conduction Mode) a more popular choice [3].

The output voltage of the BCM boost converter is normally regulated using constant on-time control [4], with an analog controller. Recent decades have seen significant improvement in microcontroller technology, with better processing power, lower cost and improved peripherals dedicated to power electronics applications. This improvement, coupled with advantages of digital control such as more design flexibility, and reduced sensitivity to temperature and process variation, has lead to widespread adoption of digital control in the design of switched-mode power supplies [5]. As a result there are many examples of digitally controlled BCM boost power supplies for PFC applications existing in literature [1], [6]–[10].

The output voltage of a PFC boost converter has a 2^{nd} harmonic ripple. To achieve good power factor the voltage compensator needs to be designed with high attenuation at the frequency of the 2^{nd} harmonic ripple and above. To achieve this high attenuation, the bandwidth of the voltage compensator will be low, typically around $10 - 15$ Hz. As a result PFC boost converters can suffer from poor voltage transients responses from load disturbances. A slow voltage transient response is a highly undesirable feature, as it can lead to high peak over shoot on the output voltage, which may exceed the output capacitor rated voltage, or cause an output voltage tracking failure which leads to a less robust and less reliable converter. To address this issue, several different approaches already exist in the literature that try to improve the dynamic performance

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of the outer voltage loop in PFC regulators. In [11] the output voltage 2nd harmonic ripple is estimated and then subtracted from the sensed output voltage, so that the voltage compensator input has no ripple component, allowing its bandwidth to be increased. Although this method provides a much faster output voltage response, it requires additional sense circuitry to sense output load current, an additional control loop and 2 high pass filters to implement. Similarly, [12] proposes a digital self-tuning comb filter that filters the ripple component from the sensed output voltage, and can adjust the filters response to changes in the line frequency. This method allows for the voltage compensator to be designed with a higher bandwidth, at the cost of a relatively small amount of computational power to implement the self-tuning filter. Dual voltage compensators are used to improve output voltage transient performance in [13], at the cost of a more complex control structure. The control scheme uses a slow voltage compensator during steady-state conditions to ensure good power factor, and switches to a fast voltage compensator during load disturbances to improve output voltage tracking. A digital controller with low computational power requirements and fast output voltage dynamics is demonstrated in [14], where the output voltage is sampled at the zero crossings of the input line voltage, removing the ripple component from the sensed output voltage signal. This combines with two voltage compensators, one with slow dynamic response to take care of steady-state operation and one with fast dynamic response to control dynamics during load disturbances. Although two voltage compensators are used in this design, computational requirements are kept low as the output voltage is sampled at such a slow rate.

The work presented in this paper presents a computationally inexpensive method to improve the output voltage dynamic performance at low input voltage, which can be used separately or be combined with the other methods mentioned above.

II. System Model

Fig. 1 shows the simplified controller structure of the interleaved BCM boost converter described in this paper. The output voltage v_o is regulated by sensing v_o using an RC circuit and the microcontroller's internal ADC. The voltage compensator calculates the average on-time of the combined phases so it can accurately track the reference voltage v_{ref}. Zero-Current-Detection (ZCD) circuitry for both phases interfaces with the PWM peripheral on the microcontroller to allow the converter to operate in BCM.

Fig. 2 shows the output voltage, inductor current and input voltage over a single line cycle. A 2nd harmonic voltage ripple exists on the output voltage. This voltage ripple can be explained by looking at the output current i_o, that flows into the output capacitor and load. Applying the power balance equation the current i_o can be described as,

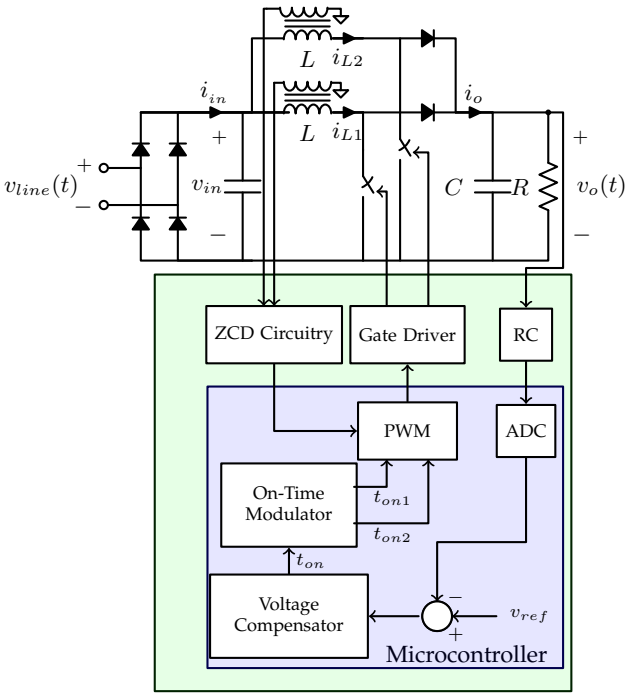


Fig. 1: Simplified circuit diagram

$$i_o = \frac{\eta v_{in} i_{in}}{v_o} \tag{1}$$

$$= \frac{\eta V_{in_{pk}} |sin(\omega t)| I_{in_{pk}} |sin(\omega t)|}{V_o} \tag{2}$$

$$= \frac{P_o}{V_o}(1 - cos(2\omega t)) \tag{3}$$

where η is the converter efficiency, $V_{in_{pk}}$ is the peak input voltage, $I_{in_{pk}}$ is the peak input current, V_o is the operating point value of the dc output voltage, ω is the frequency of the line voltage and P_o is the output power. The output current given by (3) has a dc part of P_o/V_o and a 2nd harmonic part of $-P_o/V_o\ cos(2\omega t)$. Assuming all the 2nd harmonic part flows into the output capacitor, the instantaneous output voltage can be calculated as follows;

$$v_o = \frac{1}{C}\int_{\tau=0}^{\tau=t} -\frac{P_o}{V_o} cos(2\omega\tau) d\tau + V_o \tag{4}$$

$$= V_o - \frac{1}{C}\frac{P_o}{V_o}\frac{1}{2\omega} sin(2\omega t) \tag{5}$$

Therefore the output voltage will also have a ripple with a frequency twice that of the line frequency.

Fig. 3 shows the inductor current over a single switching interval for one phase of the interleaved converter. Based on these figures the average current in one of the inductors over a single switching cycle can be written as follows,

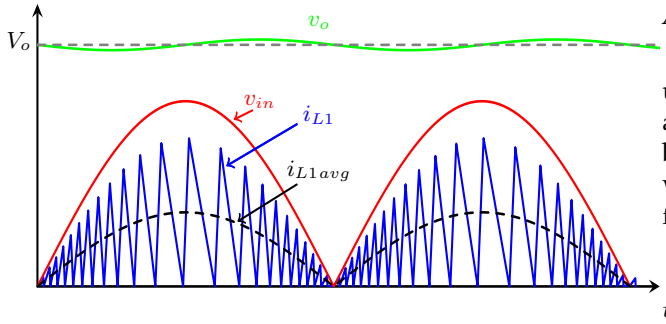


Fig. 2: Inductor current over a single line cycle.

$$i_{L1_{avg}} = \frac{t_{on}}{2L} v_{in} \tag{6}$$

where $i_{L1_{avg}}$ is the instantaneous average inductor current, t_{on} is the instantaneous on-time and v_{in} is the instantaneous input voltage.

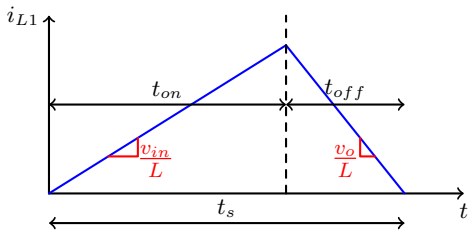


Fig. 3: Inductor current over a single switching cycle.

The total average input current i_{in} into both phases of the interleaved converter is

$$i_{in} = \frac{t_{on}}{L} v_{in} \tag{7}$$

In order to achieve near-unity power factor it is essential that i_{in} has the same shape as v_{in}. As seen from (7), this will be achieved with the BCM converter provided that t_{on} remains constant, so that i_{in} equals a constant times v_{in}. This is the basis of using constant on-time control in PFC applications.

Applying the power balance to the input and output of the interleaved boost converter shown in Fig. 1, the following expression can be written,

$$\eta v_{in} i_{in} = v_o i_o \tag{8}$$

where η is the converter efficiency. The relationship between the i_o and v_o is given in (10).

$$i_o = C\frac{dv_o}{dt} + \frac{v_o}{R} \tag{9}$$

Equations (7), (8) and (9), are the 3 governing equations that describe the system model.

A. AC Analysis

In order to design the voltage compensator to regulate t_{on} to control v_o, it is necessary to first build an accurate linear model of the system. Using the power balance expression given by (8) and combining this with (7), the current i_o can be described as a non-linear function of v_{in}, t_{on} and v_o as follows.

$$i_o = \frac{\eta}{L}\frac{v_{in}^2 t_{on}}{v_o} = f(v_{in}, t_{on}, v_o) \tag{10}$$

Linearising this function of i_o about a dc operating point, i_o can now be described as,

$$\widetilde{i_o} = g_i\widetilde{v_{in}} + k_t\widetilde{t_{on}} - \frac{\widetilde{v_o}}{R} \tag{11}$$

where the terms $g_i = \frac{2V_o}{V_{in}R}$ and $k_t = \frac{\eta V_{in}^2}{LV_o}$ are constants, defined by the dc operating point and the load resistance R. V_{in} is the average dc input voltage of the rectified sinusoid at the input of the boost converter. $V_o is the average dc value of the output voltage$. Combining (10) and (11), a full linear system model can be obtained, described by (12).

$$C\frac{d\widetilde{v_o}}{dt} + \frac{2\widetilde{v_o}}{R} = g_i\widetilde{v_{in}} + k_t\widetilde{t_{on}} \tag{12}$$

Taking the Laplace transform of (12), the open-loop system transfer functions of $\frac{V_o}{T_{on}}(s)$ can be obtained as;

$$\frac{V_o}{T_{on}}(s) = \frac{k_t}{sC + \frac{2}{R}} \tag{13}$$

It is important to point out here that the term $k_t \propto V_{in}^2$. Therefore for lower levels of input voltage the system has a lower open-loop gain and therefore will have slower output voltage tracking. Later on in this paper, a voltage compensator will be designed that varies its gain to ensure the transient response of the output voltage does not change with V_{in}, based on the fact that $k_t \propto V_{in}^2$. CCM boost converters implying average-current-mode control (ACMC) also suffer from the same effect, where a lower input voltage deteriorates the output voltage tracking. Therefore the analysis presented in this paper to improve the voltage tracking of an interleaved BCM boost converter can also be used on a CCM boost converter. For clarity, the open-loop transfer function of a CCM boost converter using ACMC is derived in the Appendix, and compared with that of an interleaved BCM boost shown in (13).

B. Model Verification

The microcontroller computation of t_{on} introduces a computational delay of a single computational cycle, which can be approximated in the Laplace domain as e^{-sT}, where T is the sampling period of the voltage compensator. Therefore the open-loop transfer function can be more accurately described by,

$$\frac{V_o}{T_{on}}(s) = \frac{k_t}{sC + \frac{2}{R}} e^{-sT} \tag{14}$$

In order to verify the accuracy of the system model, the open-loop Bode plots of the system are calculated theoretically using (14) and also measured experimentally on a 600 W BCM boost converter. The converter has an output capacitance of C = 360 µF, boost inductance of each phase is given by L = 130 µH and the voltage compensator has a sampling period of 100 µs. Fig. 4(a) shows how increasing the average input dc voltage to the converter increases the system open-loop gain. As can be seen, there is an excellent correlation between theoretical and experimental result. Similarly, Fig. 4(b) shows the impact of output power variation on the open-loop Bode plot, with experimental and theoretical results matching each other well.

III. Voltage Compensator Design

A. Open-Loop Gain

Fig. 5 presents a simplified control block diagram of the system. $C(z)$ is the z-domain transfer function of the voltage compensator. Gain k_{vo} is the combined gain of the RC filter and ADC. The voltage compensator was designed to achieve good stability and fast transient response of the output voltage, by initially designing for a phase margin ϕ_m of 45^o, and a cross-over frequency of $\omega_c = 2\pi 15$ rad/s.

The open-loop gain of the system $T_c(z)$ is given by;

$$\begin{aligned} T_c(z) &= z^{-1}C(z)Z\left\{\frac{1-e^{-sT}}{s} k_{vo} \frac{k_t}{sC + \frac{2}{R}}\right\} \\ &= z^{-1}C(z)k_t k_{vo}\frac{R}{2}\frac{1-e^{\frac{-2T}{RC}}}{z-e^{\frac{-2T}{RC}}} \end{aligned} \tag{15}$$

In the region greater than 4 Hz the open-loop system Bode plot is dominated by the output capacitor pole and can be approximated as follows;

$$\begin{aligned} T_c(z) &= z^{-1}C(z)Z\left\{\frac{1-e^{-sT}}{s} k_{vo} \frac{k_t}{sC}\right\} \\ &= C(z)k_t k_{vo}\frac{T}{C}\frac{1}{z(z-1)} \end{aligned} \tag{16}$$

B. Voltage Compensator Transfer Function

The main objective of the voltage compensator is to provide fast accurate tracking of a constant output-voltage setpoint, while still ensuring that the input current maintains near-unity PF. However, all boost converters used in PFC applications suffer from a 2nd harmonic voltage ripple on the output capacitor. To achieve good PF, the voltage compensator must have a high attenuation at frequencies near the 2nd harmonic frequency and above. This restriction greatly limits the controller bandwidth to low frequencies in the region 10-20 Hz, causing the output voltage to have a slow

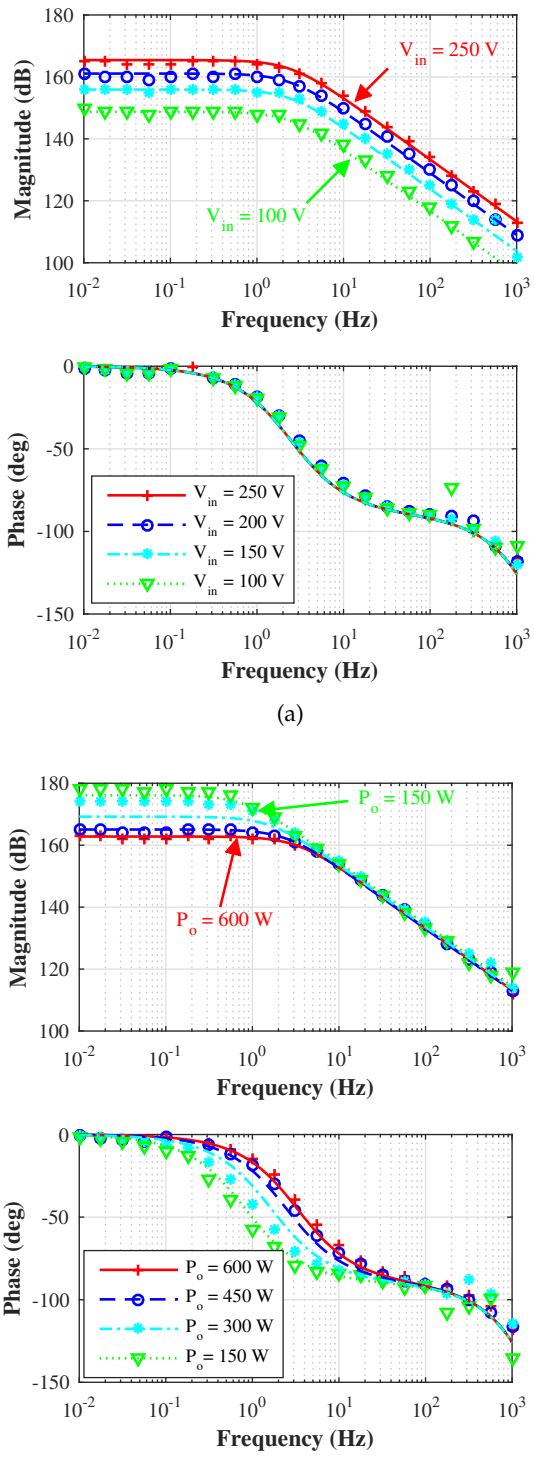


Fig. 4: Measured (x,o,*,▽) and theoretical (dashed or continuous line) open-loop Bode $\frac{V_o}{T_{on}}(s)$ plot variation (a)at P_o = 450 W with different input dc voltages, and (b)at V_{in} = 250 V with different output power P_o

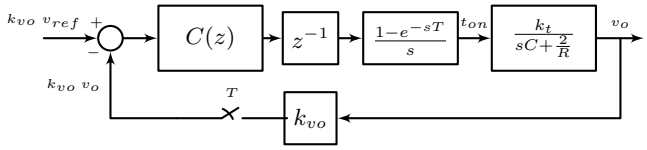


Fig. 5: Control block diagram

transient response to load disturbances.

An integral lead-lag compensator is a suitable choice of controller in the analog domain for the outer voltage loop of the BCM converter [15]. The transfer function of a type II compensator is given by (17). This controller has a pole at $s = 0$, which ensures infinite dc gain and zero steady-state error for constant voltage tracking. The controller also introduces extra phase at the cross-over frequency, to ensure the phase margin of the system is always set to a desired value.

$$C(s) = \frac{K_c}{s}\frac{1+a\tau s}{1+\tau s} \tag{17}$$

The bi-linear transformation, given by $s = \frac{2}{T}\frac{z-1}{z+1}$, is used to convert this analog transfer function to a digital compensator with similar characteristics, given in (18).

$$C(z) = k\frac{z+1}{z-1}\left(\frac{z(1+\frac{2a\tau}{T})+(1-\frac{2a\tau}{T})}{z(1+\frac{2\tau}{T})+(1-\frac{2\tau}{T})}\right) \tag{18}$$

The a and τ terms in (18) are chosen to inject 45^o of phase at the open-loop cross-over frequency by selecting $a = 0.707$ and $\tau = \frac{1}{\omega_c\sqrt{a}}$, where ω_c is the open-loop cross-over frequency.

The term k given by (17) is designed to achieve a cross-over frequency ω_c by setting the magnitude of the $Tc(z)$ to 1 at the cross-over frequency, as is done in (19).

$$|T_c(e^{j\omega_c T_s})| = 1 \tag{19}$$

Substituting T_c in (19), with the definition obtained in (16), expressions for the controller gain k can be obtained as follows;

$$k = \frac{V_o LC|e^{j\omega_c T}-1|^2\,|e^{j\omega_c T}(1+\frac{2\tau}{T})+(1-\frac{2\tau}{T})|}{V_{in}^2 k_{vo} T\,|e^{j\omega_c T}+1|\,|e^{j\omega_c T}(1+\frac{2a\tau}{T})+(1-\frac{2a\tau}{T})|} \tag{20}$$

Initially the constant k is designed to achieve a cross-over frequency of $\omega_c = 15$ Hz, at the best case operating input voltage of $V_{in} = 239$ V, for which the rms input line voltage is 265 V.

C. Open-Loop Transfer Function Variation

The variation of the uncompensated system Bode plots of $\frac{V_o}{T_{on}}(s)$ presented in Fig. 4, lead to variations in the systems compensated bode plot with changes in V_{in} and P_o.

Fig. 6(b) shows the variation in the open-loop system compensated bode plots $T_c(z)$ at different output powers. It can be seen that despite the change in output power, the systems cross-over frequency and the open-loop attenuation remain the same. Similarly, there is almost identical phase margin of 45^o for each case. This ensures there will be similar output voltage transient response, even if the operating power of the converter changes.

Fig. 6(a) shows how $T_c(z)$ changes with V_{in}. At $V_{in} = 239$ V, corresponding to an input line voltage of 265 V, $T_c(z)$ has the desired cross-over frequency of $\omega_c = 2\pi 15$ rad/s. However, as V_{in} is lowered to 77 V the cross-over frequency drops to as low as 4 Hz leading to an undesired slower output transient response. However the attenuation at the 2^{nd} harmonic frequency increases significantly. The greater attenuation at $\omega = 2\pi f_{line}$, where f_{line} is the frequency of the line voltage, leads to an improved power factor at low V_{in}. This improvement will be small, as there is already significant attenuation at this frequency to provide good power factor.

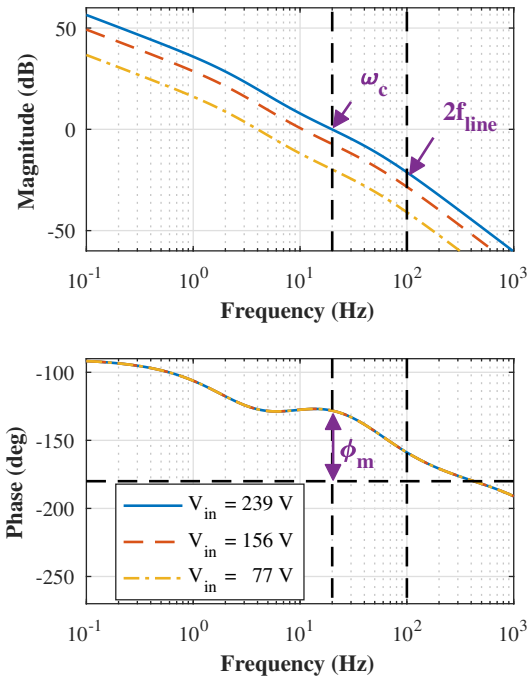
D. Adaptive Gain

To compensate for the reduced cross-over frequency at low V_{in}, an adaptive gain k_a is introduced to the voltage compensator to increase the gain based on the measured value of the V_{in}, in order to ensure the cross-over frequency of the system stays in the region $2\pi 10 \leq \omega_c \leq 2\pi 15$ rad/s. Fig. 7 shows the control block diagram with the adaptive gain term k_a. It is important to place k_a before the compensator $C(z)$ so that it multiplies the error signal which is near zero. That way, if k_a changes due to a change in input voltage, it does not disturb the input to the system as the error is near zero. If the k_a block is placed after the compensator $C(z)$, and the k_a term is stepped, this would step t_{on} and significantly disturb the system.

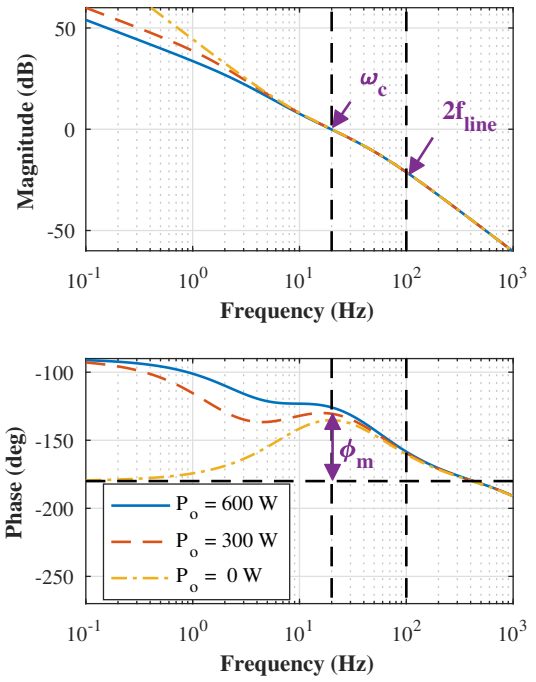
Next by re-arranging (20) to form an expression for V_{in} and initially setting the compensator gain to the value calculated for $V_{in} = 239$ V and setting $\omega_c = 2\pi 10$ rad/s. The value for $V_{in} = V_{in_1}$ for which the system will have an open-loop cross-over frequency of 10 Hz can be calculated as follows,

$$V_{in_1} = \sqrt{\frac{V_o LC|e^{j\omega_c T}-1|^2\,|e^{j\omega_c T}(1+\frac{2\tau}{T})+(1-\frac{2\tau}{T})|}{k k_{vo} T\,|e^{j\omega_c T}+1|\,|e^{j\omega_c T}(1+\frac{2a\tau}{T})+(1-\frac{2a\tau}{T})|}} \tag{21}$$

By this means, the region for $V_{in_1} \leq V_{in} < 239$ V for which the gain k will guarantees a cross-over frequency of $10 \leq \omega_c < 15$ Hz is found. The gain k required to give a $\omega_c = 15$ Hz for $V_{in} = V_{in_1}$ can then be calculated using (20). By repeating this process, and normalizing each k term calculated to the original term calculated at $V_{in} = 239$ V to obtain the gain k_a, a table can be created of the regions of V_{in} from $V_{in} = 77$ V



(a)



(b)

Fig. 6: Compensated open-loop bode plots (a) at different levels of input voltage V_{in} with $P_o = 600$ W and, (b) at different levels of output power with $V_{in} = 250$ V.

up to $V_{in} = 239$ V and the corresponding value of k_a to ensure the cross-over frequency stays in the region

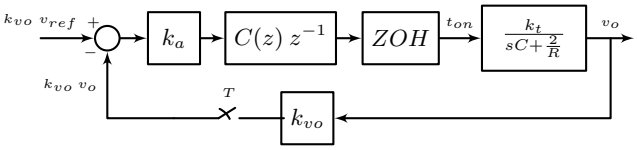


Fig. 7: Control block diagram with adaptive gain k_a

$10 \leq \omega_c < 15$ Hz as shown in Table. (I).

TABLE I: Variable gain look up table for k

V_{in} range	k_a	V_{in} range	k_a
$198 < V_{in} \leq 239$	1	$94 < V_{in} \leq 113$	4.477
$164 < V_{in} \leq 198$	1.454	$77 < V_{in} \leq 94$	6.512
$136 < V_{in} \leq 164$	2.116	$V_{in} \leq 77$	9.472
$113 < V_{in} \leq 136$	3.007		

IV. Experimental Results

A digitally-controlled 600W interleaved BCM boost converter was built, with the control implemented using a TMS320f28069 microcontroller. Fig. 8 shows the shape of v_{line}, v_o, i_{in} and i_{L1} under steady state operating conditions at $V_{line} = 230$ V and $P_o = 600$ W.

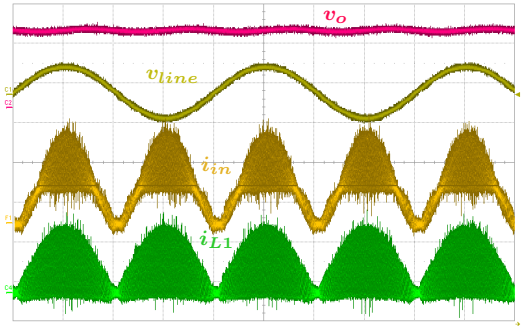


Fig. 8: Output voltage, input line voltage, input current and inductor current under normal operation at $P_o = 600$ W and $V_{line} = 230$ V (v_o: 400 V/div, v_{line}: 400 V/div, i_{in}: 5 A/div, i_{L1}: 5 A/div, Timebase: 5 ms/div).

Fig. 9 shows the transient response of v_o and the input line current i_{line} to a step in output power from P_o= 450 W to P_o= 150 W, for V_{in}= 216 V & 126 V, when the voltage compensator has a constant gain so that $k_a = 1$ for all V_{in}. It is demonstrated here that in the case V_{in}= 216 V the output voltage displays a fast transient response and low peak overshoot, however when the same loadstep is carried out at V_{in}= 126 V, v_o has a slower transient response and a larger peak overshoot.

Fig. 10 shows the transient response of v_o and i_{line} to the same load step to that in Fig. 9, when the voltage compensator has an adaptive gain so that k_a varies

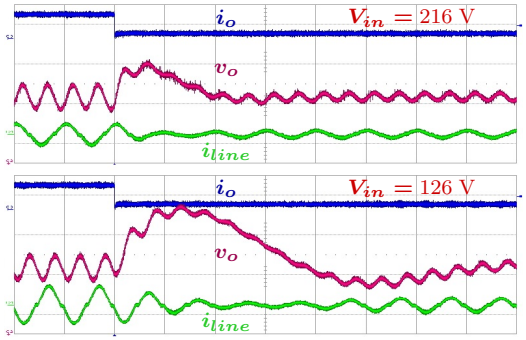


Fig. 9: Transient response of the system to load steps from 450 W to 150 W in output power, with a constant gain at V_{in} = 216 V (upper) and V_{in} = 126 V (lower). (i_o: 1 A/div, v_o: 10 V/div, i_{line}: 10 A/div, Timebase: 20 ms/div)

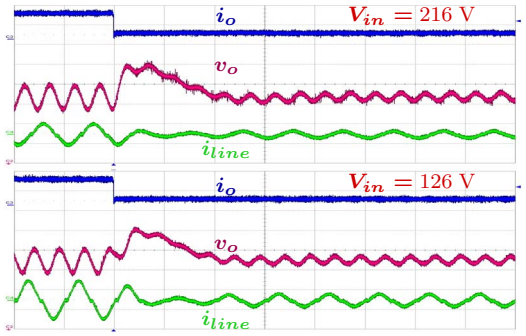


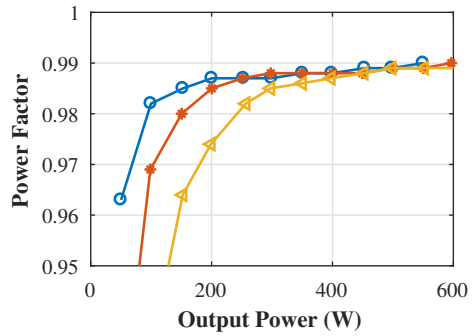
Fig. 10: Transient response of the system to load steps from 450 W to 150 W in output power, with an adaptive gain at V_{in} = 216 V (upper) and V_{in} = 126 V (lower). (i_o: 1 A/div, v_o: 10 V/div, i_{line}: 10 A/div, Timebase: 20 ms/div)

with V_{in} as per Table. I. It is demonstrated here that in both cases for V_{in}= 216 V and V_{in}= 126 V the output voltage displays a fast transient response and low peak overshoot.

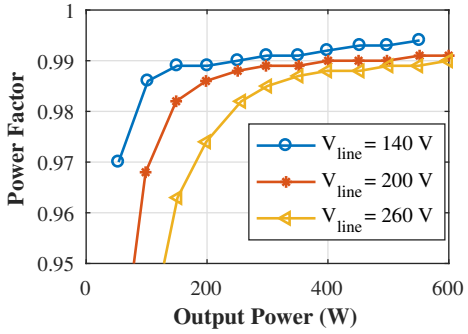
Fig. 11 shows the variation in power factor with V_{in} and P_o when the voltage compensator uses an adaptive gain, and uses a constant gain. Here it can be seen that using the adaptive gain reduces the power factor at low V_{in}, however the worst case power factor which occurs at $V_{line} = 260V_{rms}$ stays the same in both cases.

V. Conclusion

This paper presents a digital control strategy that controls the output voltage for an interleaved BCM PFC converter, with fast transient response at low input voltage. Small-signal analysis is carried out to describe the relationship between on-time and output voltage, in order to build an accurate model of the system. The system model is verified experimentally



(a)



(b)

Fig. 11: PF variation with P_o and V_{in} using (a) an adaptive gain, and (b) a constant gain.

by measuring the system open-loop Bode plots at different dc operating points. Based on this system model a voltage compensator is designed to regulate the converters output voltage. The voltage compensator design is improved by using an adaptive gain to increase the open-loop system cross-over frequency at low input voltage. The performance of the designed voltage compensator is verified experimentally with and without an adaptive gain by measuring the systems transient response to load disturbances at different levels of input voltage.

Appendix

Single-channel CCM boost PFC power supplies are usually controlled using a combination of a fast inner current loop to control the input current, and a slow outer voltage loop to control the output voltage, as is shown in Fig. 12. The inner loop works by sensing the input and comparing it to a reference signal i_{ref}, which is generated by multiplying the input voltage by a constant k and a second term v_c the output of the voltage compensator in the outer control loop. The current compensator is designed to calculate the appropriate duty cycle d to ensure i_{in} tracks i_{ref}.

If it is assumed that i_{in} tracks i_{ref} perfectly, then i_{in} will be given by;

$$i_{in} = kv_{in}v_c \tag{22}$$

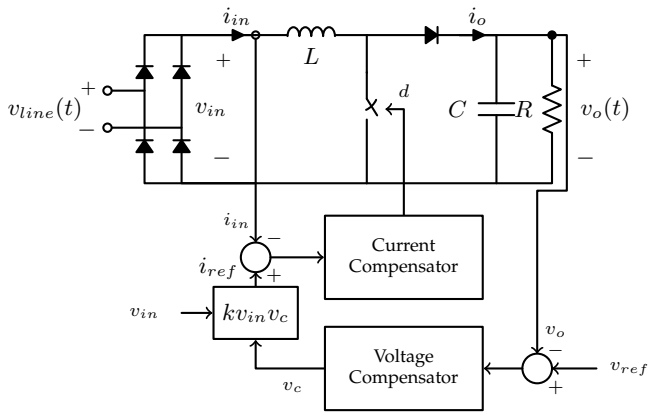


Fig. 12: CCM Boost converter with ACMC.

Combining (22) with the power balance equation $\eta v_{in} i_{in} = v_o i_o$, where η is the boost converter efficiency, v_o is the output voltage, and i_o is the time-averaged output current flowing through the boost diode, the following non-linear equation can be written to describe i_o,

$$i_o = \eta k \frac{v_{in}^2 v_c}{v_o} = f(v_{in}, v_c, v_o) \tag{23}$$

As the current i_o flows into an RC load, it can also be described as follows,

$$i_o = C\frac{dv_o}{dt} + \frac{v_o}{R} \tag{24}$$

Combining (23) and (24), a full linear system model can be obtained, described by (12).

$$C\frac{d\widetilde{v_o}}{dt} + \frac{2\widetilde{v_o}}{R} = g_i\widetilde{v_{in}} + k_t\widetilde{v_c} \tag{25}$$

where the terms $g_i = \frac{2V_o}{V_{in}R}$ and $k_t = \frac{\eta k V_{in}^2}{V_o}$ are constants, defined by the DC operating point and the load resistance R. Taking the Laplace transform of (25), the open-loop system transfer functions of $\frac{V_o}{V_c}(s)$ can be obtained as;

$$\frac{V_o}{V_c}(s) = \frac{k_t}{sC + \frac{2}{R}} \tag{26}$$

This open-loop transfer function is almost identical to the open-loop transfer function obtained in (13) for the interleaved BCM converter, except that the term k_t is different. More importantly however, $k_t \propto V_{in}^2$ for both cases. Therefore, the methods described in this paper to improve the transient response of the output voltage when at low input voltage can also be applied to a CCM boost converter employing ACMC.

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