FAILURE ANALYSIS OF A BIPOLAR INTEGRATED CIRCUIT

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ABSTRACT

The research of failure analysis for integrated circuits can improve the reliability. Based on one failed circuit, do the analysis which including eletrical parameter test, chip surface check, schematic diagram and layout analysis,and find the failure reason, then use simulation to verify the analized conclusion. Finally, throw out some effective ways to avoid this kind of failure that might happen again, which is helpful for improving the reliability of integrated circuits.

INTRODUCTION

Nowadays people have higher requirement on the products' reliability, and the research of the reliability about the product becomes more and more important[1].

Integrated circuit failure analysis is extremely important for improving the reliability.With the raise of integration and shrinking of process dimensions, the difficulties faced by failure analysis are also gradually increasing[2].New failure analytic technologies and instruments are developed and applied to the field of failure analysis for electronic components, failure analysis can improve line yield, get failed sample root cause[3].

This paper shows out a whole process of failure analysis. According to the results of testing, considering the schematic and layout, find out the reason of the failure.

TEST OF FAILURE CIRCUIT

Electrical Parameter Test

One circuit suddenly output an abnormal signal, first is to test the eletrical parameter and compared with the normal one.The results shown in Table I.

TABLE I. ELECTRICAL PARAMETER TEST

Test	Eletrical Parameter			
	Consumption Current	***Max Frequency***	***Pin4 Gain***	***Pin5 Gain***
Unit	mA	MHz	dB	dB
Sample	1.9	156	13.2	13.5
Failure	2.0	157	-12.5	19.2

The circuit is an amplifier, table I shows that its output gain is not normal any more.Somewhere inside of the circuit must have already damaged, in order to locate the failure position, we must combine the testing results with schematic diagram analysis.It is shown in Figure 1.

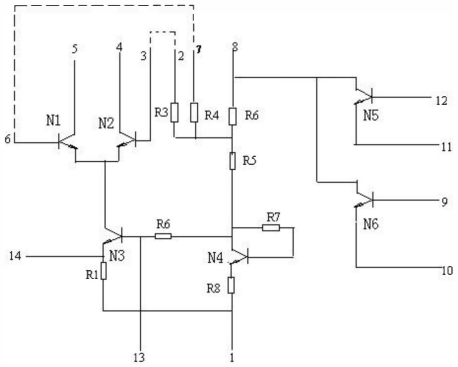

Figure 1: Schematic diagram

The pin 4, pin 5 are respectively two collectors of two NPN transistors, from the testing results, the pin 4 has almost no gain signal, meanwhile, the pin 5 gain is larger than the normal one, so we can come to a conclusion: the N2 transistor in the failure circuit is shut off due to some unpredictable reason .The current through N3 should be equal divided by N1, N2, but now , all through N1, resulting in pin 5 gain larger than normal output.

Working Point Test

We want to know why N2 is shut off unnormally.Test static working point of this circuit in testing system by a multimeter, the results as shown in Table II.

TABLE II. STATIC WORKING POINT TEST

Test	Static Working Point(7 pins)						
	2	***3***	***4***	***6***	***7***	***13***	***14***
Sample	4.2	4.2	12.4	4.2	4.2	1.8	1.0
Failure	0.08	0.08	14.9	2.6	2.6	1.3	0.6

The obvious difference is the potential of pin 2 and pin 3 have only 0.08V in contrast to the normal one's 4.2V, which is not high enough to switch on the BE junction.

Impedance Test

Another method is to test the impedence from each pin to ground, and the results shown in Table III.

TABLE III. IMPEDANCE TO GROUND TEST

Test	Impedance to Ground(7 pins)						
	2	***3***	***4***	***6***	***7***	***13***	***14***
Sample	1M	∞	∞	∞	1M	1M	295
Failure	1M	**100**	∞	∞	1M	1M	293

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The only difference is pin 3, the impedance should be infinite, but the failure circuit has showed a small resistance. The resistance shows in schematic as in Figure 2.

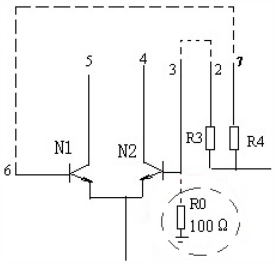

Figure 2: Schematic diagram with small resistance

We can guess that this small resistance is the most fundamental cause of circuit failure.But analysis is not enough, we need simulation to illustrate if it is the cause of gain reduction and N2's shutdown.

Simulation Validation

Simulated circuit is according to the testing system .First, simulate the gain of pin 4, pin 5 under normal conditions, and the results are shown in Figure 3.

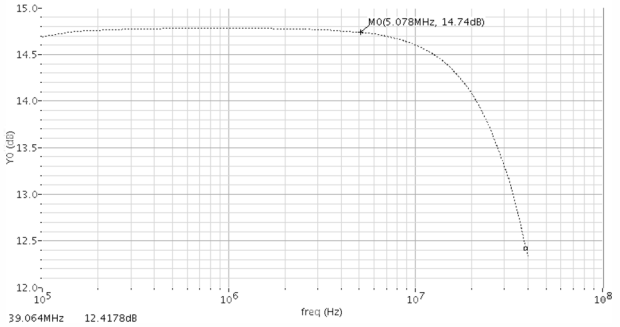

Figure 3: Normal pin4(5) gain simulation

Due to the ideality of simulation and the symmetry of pin 4 and pin 5, the two output curves are completely overlap.The gain is about 14.7dB at 5MHz frequency.

Then we connect one resistor of 100Ohm between pin 3 and the ground, and the simulation results shown in Figure 4.

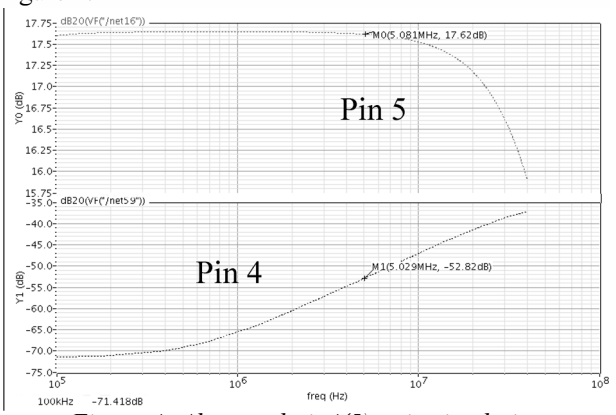

Figure 4: Abnormal pin4(5) gain simulation

We can see from Figure 4, after this small resistance connected between pin 3 and ground, the gain of pin 5 is about 17.6dB while the gain of pin 4 is -52.8dB which is negative gain, nearly no output.The results are consistent to the testing results of failure circuit.

Through the above analysis and simulation, we confirm that the failure reason is the small resistance between pin 3 and ground.

RESISTANCE LOCATION

Chip Surface Check

We broke the circuit's tube and check the surface of the chip, the photo shows that there is no abnormal traces. We must do a further analysis.

Analysis And Positioning

According to the analysis of the chip structure and layout, there are three possible reasons that may cause the small resistance:

a、N2, N3 transistor penetrate to the ground;

b、BC, CS junction of N2 are penetrated;

c 、 Somewhere between aluminum line, which connect pin 3 and the base of N2, and the oxide layer which is isolation , breakdown occurs.

The fault tree is shown in Figure 5.

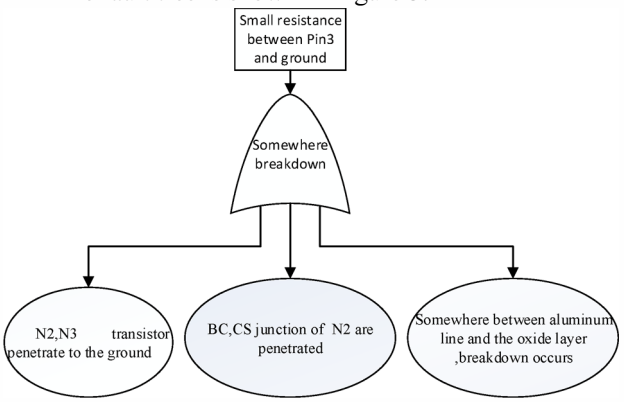

Figure 5: Fault tree

We must exlude two reasons that are not established.

Possibility A： N2, N3 transistor penetrate to the ground;

In this case, the impedance of pins (such as 2 feet, 4 feet, 7 feet, 13 feet) that through N2, N3 to the ground would be a small resistance, but according to the results shown in Table II, these pins had no obvious difference. In addition, the branch has R1 of 300Ω, which is greater than 100 Ω, thus excluding this possibility.

Possibility B： BC, CS(collector to substrate)junction of N2 are penetrated;

If this case is tenable, a conductive path is established between the pin 3→base of N2 → N2 →collector of N2 →substrate, then the collector of N2 (pin 4) to ground would shows 100 ohm resistor or even smaller, but It's not.

Thus excluding possibility b.

Possibility C：Somewhere between aluminum line which connect pin3 and the base of N2, and the oxide layer which is isolation, breakdown occurs;

Excluding the former two possibilities, only this one can be established, and this possibility cause only pin 3 connecting a small resistance to ground.

PROCESS ANALYSIS

The former analysis come to the conclusion of the reason of failure, now we must analyse how this small resistance produced.

In integrated circuit processing, usually using a silicon oxide layer which acts as an insulating layer, a protective layer, as shown in Figure 6.

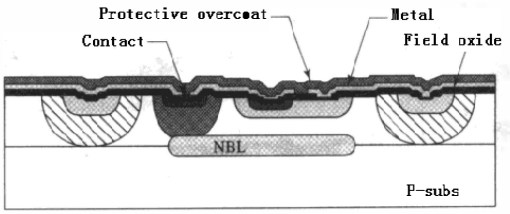

Figure 6: NPN transistor sectional view[4]

The silicon oxide layer is mainly composed of SiO_2, its structure is the tetrahedral structure consists of a Si atom surrounded by four oxygen atoms.

In the process, due to the inevitable small particles existing in the air, when they fall on the surface of silicon wafer, they will attach, in the process of oxide layer, there will be pinhole with the same size of these particles in the particle position, as shown in Figure 7.

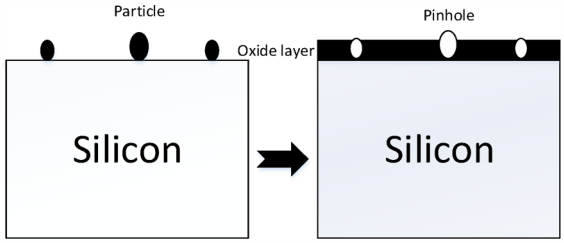

Figure 7: Pinhole produced(SiO2 process)

Except process of SiO_2 may produce pinhole due to the particle, another possibility of pinhole is in the process of lithography corrosion. If the photoresist at the protection region of the SiO_2 has pinhole, it also can produce the pinhole, as shown in Figure 8.

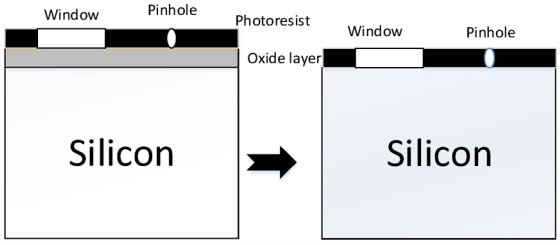

Figure 8: Pinhole produced(Lithography corrosion)

When the pinhole of oxide produced, its voltage capacity will reduce, even lower than the normal working voltage of the circuit, which causes easy breakdown of the ciucuit.

According to the former analysis, if somewhere in the SiO_2 layer between the aluminum wire which connect pin 3 and the base of N2, and the substrate has pinhole, the breakdown voltage will reduce, when this circuit is working in the normal voltage condition, it could be broke down and then produce a small resistance between pin 3 and the ground. In this case, the surface of the chip have no obvious traces.We can only get the conclusion by testing and analysis.

CONCLUSION

The reason of this failure circuit is because some pinhole produced in the SiO_2 layer, causes its low breakdown voltage, when it's working, some unpredictable large voltage condition causes the breakdown, then produced a small resistance between pin 3 and the ground, the circuit is broken.

In order to avoid this kind of failure happening again and improve product's reliability, we should upgrade the cleanliness level of the processing line, decrease the amount of particles in the air, reduce the risk of producing pinhole on the chip, so that the elecronic components could maintain the normal withstand voltage and reliability.

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