A Dynamic Model of Switched-Capacitor Power Converters

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***Abstract*—Switched-capacitor (SC) converters are frequently used for low-power applications that require little or no output regulation. Previous work has established static SC converter models, essentially composed of an ideal transformer (with turns ratio determined by the topology) and an output resistance that varies with component choices, switching frequency, and duty ratio. In this paper, the static model is expanded to include the dynamic response to the input voltage and output current changes. The dynamic model is particularly important in systems that experience large output power transients, such as low-power systems that enter and exit sleep modes. For applications that are only concerned with input–output behavior, a reduced-order model that neglects internal dynamics is derived. The dynamic model is validated with both simulations and experimental results.**

***Index Terms*—DC-DC power converters, state-space methods, switched capacitor circuits.**

I. Introduction

SWITCHED-CAPACITOR (SC) converters range from simple voltage doublers to highly complex topologies, such as the Fibonacci topology (known to achieve maximum gain for a given number of capacitors) [1], [2]. Because of their high efficiency and lack of inductors, SC converter applications are growing, especially in fully integrated systems [3], [4]. An SC converter is typically used for an application that requires little or no regulation, because the most common regulation methods either require dynamic changes in the topology [5]–[7] or lead to increased losses [8]–[11]. In previous works, a variety of static models have been derived corresponding to the simplified model shown in Fig. 1, an ideal transformer with output resistance [12]–[17]. This study builds on the methodology in [13], which converts the set of continuous-time dynamic equations corresponding to the set of switching modes into a discrete-time model. To find a static model, the method in [13] finds the steady-state solution to the discrete-time model. One key advantage is the ability to automate this method, as shown in [18].

In this paper, two dynamic models are derived. The first model uses essentially an intermediate step in [13] directly, without continuing on to the steady-state solution. This full-order dynamic model captures all of the internal dynamics, which may be important in certain situations (such as start-up or fault conditions). However, in most situations, input–output (I/O) small-signal behavior is more relevant. Therefore, a reduced-order model is derived from the full-order model and used to find such I/O characteristics as output impedance and audio susceptibility. The method applies directly to quasi-steady-state converters, that is, unregulated converters with fixed switching frequency, fixed duty ratio, and small disturbances in the source and load. As compared to other dynamic models, such as [12], the proposed model may be readily derived from a netlist of an arbitrarily complex SC converter using automated methods. Also, the proposed model is more convenient to use for quasi-steady-state converters, which compose the majority of applications (e.g., [19] and [20]), than the model used for high-performance variable-structure control in [21]. In the sections to follow, the model is derived generically, simulation results are given for the three-stage and five-stage Fibonacci converters, and experimental results are given for a five-stage Fibonacci converter. These results demonstrate the ability of the proposed model to match the performance of a complex SC topology.

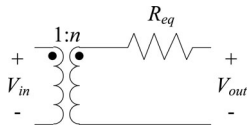

Fig. 1. Standard static model of an SC converter.

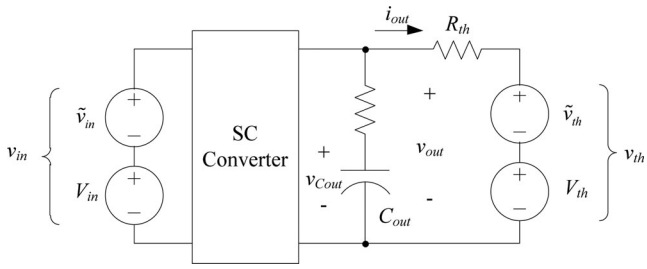

Fig. 2. SC converter with output stage and load.

II. Full-Order Dynamic Model Derivation

Without loss of generality, the load is modeled as a Thevenin equivalent, as shown in Fig. 2. Some loads are more easily modeled in Norton form, but a Norton–Thevenin conversion is always possible. Similarly, the Thevenin equivalent voltage and resistance could be positive, negative, or zero to represent

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different load types. Therefore, the circuit of Fig. 2 is taken to represent all of the important small-signal behavior.

Following the conceptual approach of [13], the vector of capacitor currents, **i**, is computed from the vector of capacitor voltages, **v**, using

$$\mathbf{i} = \mathbf{C}\dot{\mathbf{v}} \tag{1}$$

where **C** is a diagonal matrix composed of the capacitor values. The vectors **i** and **v** contain only the currents and voltages of the internal capacitors, inside the "SC Converter" box of Fig. 2. To incorporate the extra elements on the output terminals, shown in Fig. 2, the vectors and matrices are augmented so that

$$\hat{\mathbf{i}} = \begin{bmatrix} \mathbf{i} \\ i_{C\mathrm{out}} \end{bmatrix}, \ \hat{\mathbf{v}} = \begin{bmatrix} \mathbf{v} \\ v_{C\mathrm{out}} \end{bmatrix}, \ \hat{\mathbf{C}} = \begin{bmatrix} \mathbf{C} & 0 \\ 0 & C_{\mathrm{out}} \end{bmatrix}. \tag{2}$$

With these updated definitions, and with an input vector $\mathbf{u} = \begin{bmatrix} v_{\mathrm{in}} & v_{\mathrm{th}} \end{bmatrix}^T$, Kirchhoff's current and voltage laws (KCL and KVL) may be applied in each switching state, indexed $j \in \{1, \ldots, m\}$. In the examples to follow, and in most SC converters $m = 4$, with two active states separated by two idle states (switch deadtimes). The equations that result from KCL and KVL can be assembled into m matrix equations of the form

$$\hat{\mathbf{E}}_j \hat{\mathbf{i}} + \hat{\mathbf{F}}_j \hat{\mathbf{v}} + \hat{\mathbf{G}}_j \mathbf{u} = \mathbf{0}. \tag{3}$$

The caret is used to distinguish the augmented vectors and matrices that account for output capacitance from the vectors and matrices given in [13]. Equations in the form of (3) may be found automatically from a netlist using the method in [18], which was adapted from [22].

As in the static analysis in [13], each equation of the form of (3) may be converted to a continuous-time dynamic model of the general form

$$\frac{d\hat{\mathbf{v}}}{dt} = \hat{\mathbf{A}}_j \hat{\mathbf{v}} + \hat{\mathbf{B}}_j \mathbf{u} \tag{4}$$

and then converted to a discrete-time dynamic model using the conventional method detailed in [23] and implemented in MATLAB as `c2d`. This process results in m models of the form

$$\hat{\mathbf{v}}\left[k+1\right] = \hat{\mathbf{\Phi}}_j \hat{\mathbf{v}}\left[k\right] + \hat{\mathbf{\Gamma}}_j \hat{\mathbf{u}}\left[k\right]. \tag{5}$$

The sample time corresponding to the jth dynamic model is the time spent in that switching mode, typically represented as a fraction, D_j, of the total switching period T. The m dynamic models may be combined into a single dynamic model that represents the discrete-time dynamics with a sample time of T

$$\begin{aligned} \hat{\mathbf{v}}\left[k+1\right] &= \hat{\mathbf{\Phi}}\hat{\mathbf{v}}\left[k\right] + \hat{\mathbf{\Gamma}}\hat{\mathbf{u}}\left[k\right] \\ \hat{\mathbf{\Phi}} &= \hat{\mathbf{\Phi}}_m \hat{\mathbf{\Phi}}_{m-1} \cdots \hat{\mathbf{\Phi}}_1 \\ \hat{\mathbf{\Gamma}} &= \hat{\mathbf{\Gamma}}_m + \hat{\mathbf{\Phi}}_m(\hat{\mathbf{\Gamma}}_{m-1} + \hat{\mathbf{\Phi}}_{m-1}(\hat{\mathbf{\Gamma}}_{m-2} \\ &\quad + \hat{\mathbf{\Phi}}_{m-2}(\hat{\mathbf{\Gamma}}_{m-3} + \cdots))). \end{aligned} \tag{6}$$

This model may be used directly and captures all of the internal dynamics of the SC converter. To extend this method to regulated converters, a numerical perturbation in the set of duty ratios, D_j, or switching period, T, could be performed according to the particular method of regulation.

The system output, y, is the output voltage, which is nearly equivalent to $v_{C\mathrm{out}}$. Either the corresponding entry in $\hat{\mathbf{v}}$ may be used, or (3) may be solved for $\hat{\mathbf{v}}$ as a function of $\hat{\mathbf{i}}$ and **u**. Whichever choice is made, the result is an output equation of the form

$$y = \mathbf{P}\hat{\mathbf{v}} + \mathbf{Q}\mathbf{u}. \tag{7}$$

P and **Q** are used to distinguish from the capacitor matrix and duty ratios. Both are row vectors. For example, if $v_{C\mathrm{out}}$ is used directly, $\mathbf{P} = \begin{bmatrix} 0 \cdots 0 & 1 \end{bmatrix}$ and $\mathbf{Q} = \begin{bmatrix} 0 & 0 \end{bmatrix}$.

III. I/O Model Derivation

In most cases, the internal dynamics of the SC converter are of limited interest. Rather, the designer is concerned with I/O behavior, such as output impedance and audio susceptibility. The order of the model in (6) is equal to the number of capacitors, including the output capacitor. For a simple voltage doubler, perhaps this is acceptable. For something more complex, such as a high-gain ladder converter or Fibonacci converter, such a high-order model is difficult to work with, and in fact provides limited value to the designer.

Because the circuit is composed entirely of capacitors and resistors, all of the eigenvalues of Φ are real. A single, dominant eigenvalue, λ, primarily determines the transient behavior of the circuit. For a discrete-time system, the dominant eigenvalue is the one closest to the unit circle, which in this case is the largest (real) eigenvalue. Therefore, the high-order model may be reduced to a simple first-order model of the form

$$y\left[k+1\right] = \lambda y\left[k\right] + (1-\lambda)\left(\alpha_1 u_1\left[k\right] + \alpha_2 u_2\left[k\right]\right). \tag{8}$$

The gains on the input variables may be found from the dc gain of the system

$$\begin{bmatrix} \alpha_1 & \alpha_2 \end{bmatrix} = \mathbf{Q} + \mathbf{P}\left(\mathbf{I} - \mathbf{\Phi}\right)^{-1}\mathbf{\Gamma} \tag{9}$$

where **I** is an identity matrix with the same dimensions as $\mathbf{\Phi}$. The discrete-time model may be readily transformed into a Laplace-domain model of the form

$$\begin{aligned} Y\left(s\right) &= \frac{\alpha_1 a}{s+a}U_1\left(s\right) + \frac{\alpha_2 a}{s+a}U_2\left(s\right) \\ a &= -\frac{\ln\left(\lambda\right)}{T}. \end{aligned} \tag{10}$$

The two terms in (10) may be transformed into audio susceptibility and output impedance. Audio susceptibility, which reflects the small-signal change in the output voltage, $\tilde{v}_{\mathrm{out}}$, due to a small-signal change in the input voltage, $\tilde{v}_{\mathrm{in}}$, is the first term directly

$$\frac{\tilde{v}_{\mathrm{out}}}{\tilde{v}_{\mathrm{in}}} = \left.\frac{Y}{U_1}\right|_{U_2=0} = \frac{\alpha_1 a}{s+a}. \tag{11}$$

The ideal voltage gain, as determined by the SC topology, is absorbed within the audio susceptibility.

Output impedance cannot be found as easily, but may be derived from Fig. 2. The small-signal change in output current, $\tilde{i}_{\mathrm{out}}$, is determined by the change in voltage drop across the

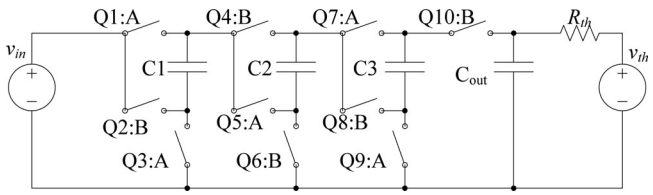

Fig. 3. Three-stage Fibonacci SC converter.

Thevenin equivalent load resistance

$$\tilde{i}_{\rm out} = \left.\frac{\tilde{v}_{\rm out} - V_{\rm th}}{R_{\rm th}}\right|_{\tilde{v}_{\rm in}=0} = \left.\frac{Y - U_2}{R_{\rm th}}\right|_{U_1=0}. \quad (12)$$

The output impedance of the SC converter itself is then determined by dividing the change in output voltage by the change in output current and simplifying

$$Z_{\rm out} = -\frac{\tilde{v}_{\rm out}}{\tilde{i}_{\rm out}} = \frac{\alpha_2 a R_{\rm th}}{s + (1-\alpha_2)\, a}. \quad (13)$$

This form may not be used for true voltage source loads ($R_{\rm th} = 0$) or true current source loads ($R_{\rm th} \to \infty$), but may be used for most practical loads. This form also provides an approximation to the equivalent output resistance $R_{\rm eq}$

$$R_{\rm eq} \approx Z_{\rm out}|_{s=0} = \frac{\alpha_2 R_{\rm th}}{1-\alpha_2}. \quad (14)$$

The approximation in (14) will be compared to the results in [13] in the simulation study given below. Although it seems counterintuitive that $R_{\rm th}$ (characteristic of the load) factors into $R_{\rm eq}$ (characteristic of the converter), $R_{\rm th}$ is also absorbed into α_2 and the effects nearly cancel out.

IV. Example: Fibonacci Converter

To make the abstract analysis from above more concrete, a three-stage Fibonacci converter with a topology gain of 5 has been analyzed completely. The circuit is shown in Fig. 3. For convenience, all switches are assumed to be identical, with on-state resistance $R_{\rm sw} = 10\ {\rm m}\Omega$, and all capacitors are assumed to be identical, with capacitance of 100 μF and equivalent series resistance of $R_c = 20\ {\rm m}\Omega$. The circuit operates in four states: active with switches labeled "A" turned ON, idle, active with switches "B" turned ON, and idle again. When the "A" switches turn ON, C1 charges to approximately $V_{\rm in}$ through Q1 and Q3. When the "B" switches turn ON, the input and C1 are in series (via Q2) and charge C2 to 2 $V_{\rm in}$ through Q4 and Q6. When the "A" switches turn ON again, C3 is charged to 3 $V_{\rm in}$. When the "B" switches turn ON again, C2 and C3 are in series and charge $C_{\rm out}$ to 5 $V_{\rm in}$. Each additional stage increases the gain according to the Fibonacci sequence: 1, 2, 3, 5, 8, 13, 21,.... As shown in [1], this topology provides the maximum voltage gain for a given quantity of capacitors.

As is typical in a real application, the duty ratios for modes A and B (numbered 1 and 3 according to the switching sequence) are assumed to be equal and the duty ratios for the two idle modes (numbered 2 and 4) are assumed to be equal. The matrices corresponding to (3) are given symbolically in Table I. The output voltage will be sampled at the end of the second idle time, so the output equation is

$$y = v_{\rm out} = \begin{bmatrix} 0 & 0 & 0 & \dfrac{R_{\rm th}}{R_c + R_{\rm th}} \end{bmatrix} \hat{\mathbf{v}} + \begin{bmatrix} 0 & \dfrac{R_c}{R_c + R_{\rm th}} \end{bmatrix} \mathbf{u}. \quad (15)$$

During the idle time, the switching capacitors are disconnected, and only the output capacitor changes voltage. Therefore, as indicated in Table I, there is only one active state variable. When composing the discrete-time model for this mode in the form of (5), additional information is needed for the remaining states. Because the other capacitor voltages do not change, the continuous-time model for the idle mode is

$$\frac{d\hat{\mathbf{v}}}{dt} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \alpha \end{bmatrix} \hat{\mathbf{v}} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ \beta_1 & \beta_2 \end{bmatrix} \mathbf{u}$$

$$\alpha = -\left(1/C_{\rm out}\right)\left(1/E_2\right) F_2 = -\frac{1}{C_{\rm out}\,(R_c + R_{\rm th})}$$

$$\begin{bmatrix} \beta_1 & \beta_2 \end{bmatrix} = -\left(1/C_{\rm out}\right)\left(1/E_2\right) \mathbf{G}_2 = \begin{bmatrix} 0 & \dfrac{1}{C_{\rm out}\,(R_c + R_{\rm th})} \end{bmatrix}. \quad (16)$$

The parameters, α, β_1, and β_2, are found from the matrices given in Table I according to the standard method in [13]. To complete the model in (16), the **A** and **B** matrices must be the same dimensions as for the other operating modes, so zeros are added, reflecting the fact that the first three capacitors (besides the output capacitor) are disconnected. Following the methodology in [13], the continuous-time model of (16) may be converted to a discrete-time model, and the remainder of the aforementioned derivation still applies.

The reduced-order model was calculated using MATLAB, and a simulation was constructed using PLECS, a blockset for MATLAB/Simulink. The input voltage steps from 1.0 to 1.2 V, and then the Thevenin equivalent load is stepped from 0 to 3 V, with constant $R_{\rm th} = 10\,\Omega$. For a switching frequency of 100 kHz, the dominant discrete-time eigenvalue is 0.9488, corresponding to a continuous-time pole at 5.261 krad/s. The discrete-time model is

$$y[k+1] = 0.9488 y[k] + 0.05124\left(4.3828 v_{\rm in}[k] + 0.1234 V_{\rm th}[k]\right). \quad (17)$$

The audio susceptibility is

$$\frac{\tilde{v}_{\rm out}}{\tilde{v}_{\rm in}} = \frac{23.06 \times 10^3}{s + 5.261 \times 10^3} = \frac{4.3828}{1 + s\,(190 \times 10^{-6})}. \quad (18)$$

The output impedance, in Ω, with a switching frequency of 100 kHz is

$$Z_{\rm out} = \frac{6.4932 \times 10^3}{s + 4.6111 \times 10^3} = \frac{1.4082}{1 + s\,(216.9 \times 10^{-6})}. \quad (19)$$

Taking the dc value of $Z_{\rm out}$, the equivalent resistance of the SC converter is approximately 1.4082 Ω. Using the model of

TABLE I
MATRICES FOR ACTIVE AND IDLE MODES OF THREE-STAGE FIBONACCI CONVERTER

Mode A	$\mathbf{E}_1 = \begin{bmatrix} -(2R_{sw}+R_c) & R_{sw} & 0 & 0 \\ (R_{sw}+R_c) & 0 & -(3R_{sw}+2R_c) & 0 \\ 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & -(R_c+R_{th}) \end{bmatrix}$	$\mathbf{F}_1 = \begin{bmatrix} -1 & 0 & 0 & 0 \\ 1 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 \end{bmatrix}$	$\mathbf{G}_1 = \begin{bmatrix} 1 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 1 \end{bmatrix}$
Mode B	$\mathbf{E}_3 = \begin{bmatrix} (2R_{sw}+R_c) & -(R_{sw}+R_c) & 0 & 0 \\ 0 & (R_{sw}+R_c) & (2R_{sw}+R_c) & -R_c \\ 1 & 1 & -1 & 0 \\ 0 & 0 & -R_{th} & -(R_c+R_{th}) \end{bmatrix}$	$\mathbf{F}_3 = \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 1 & 1 & -1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 \end{bmatrix}$	$\mathbf{G}_3 = \begin{bmatrix} 1 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 1 \end{bmatrix}$
Idle	$E_2 = E_4 = R_c + R_{th}$	$F_2 = F_4 = 1$	$\mathbf{G}_2 = \mathbf{G}_4 = [0 \quad -1]$

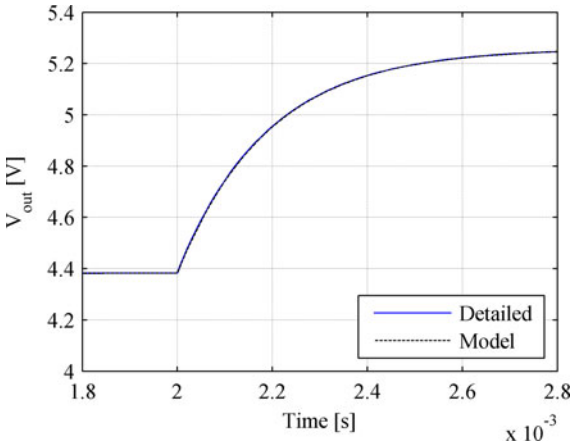

Fig. 4. Detailed simulation and model response to step in $v_{\rm in}$.

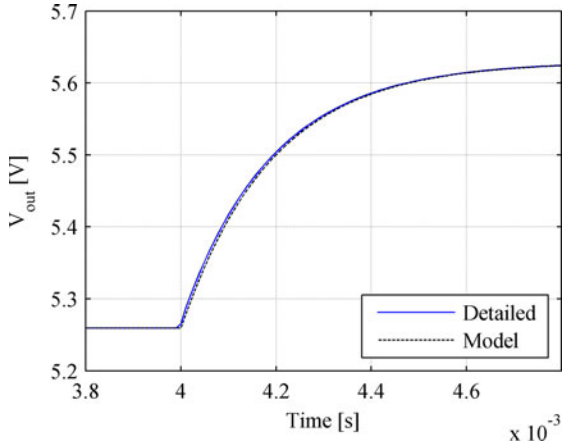

Fig. 5. Detailed simulation and model response to step in $v_{\rm th}$.

[13], the equivalent resistance at this switching frequency is 1.4045 Ω, indicating an error of 0.26%. Given the usual accuracy of component values, this degree of precision is adequate for virtually all applications.

With an output resistance of 1.4082 Ω and a load of 10 Ω, there is a voltage-divider effect after the ideal gain of the converter (which is 5). Therefore, the expected ratio between static input and output voltage is

$$\frac{v_{\rm out}}{v_{\rm in}} = (5)\left(\frac{10}{10+1.4082}\right) = 4.3828 \tag{20}$$

which is equal to α_1 in (17).

The accuracy of the reduced-order dynamic model is most apparent in time-domain simulations. Figs. 4 and 5 show the results of the detailed, switching simulation superimposed on a simulation of the reduced-order model (17), in response to a step change in the input voltage (see Fig. 4) and Thevenin equivalent load voltage (see Fig. 5). The model is nearly indistinguishable from the detailed simulation, with a maximum difference of 6 mV in Fig. 4 and 9 mV in Fig. 5.

To verify the output impedance with simulation, the Thevenin equivalent load was augmented with a sinusoidal perturbation voltage, shown as $\tilde{v}_{\rm th}$ in Fig. 2. Using analysis tools built into PLECS, the frequency of the perturbation was swept and output impedance calculated. The results are compared to the calculated impedance from (19) in Fig. 6. The magnitudes are nearly indistinguishable, and the phases match well at low frequencies. Phase diverges at high frequency because the model was derived from a discrete-time model and the actual system is continuous time. If zero-order holds are added to the perturbation source and measurement, phase matches precisely across the frequency range as indicated in Fig. 6. The frequency of perturbation was limited to 1/10th of the switching frequency, above which there may be interactions between the perturbation and switching action that are not included in this model.

In the preceding discussion, a three-stage Fibonacci converter was used because the matrices are small enough to show and discuss in detail. However, the experimental converter in the next section is a five-stage Fibonacci converter. A simulation and a model were constructed using the parameters of the experimental converter. Time-domain and impedance results are shown in Figs. 7–9. The small-signal models of the five-stage converter are

$$y[k+1] = 0.9645y[k] + 0.4354v_{\rm in}[k] + 0.00201v_{\rm th}[k] \tag{21}$$

$$Z_{\rm out} = \frac{6.0293}{1+s\,(586.5\times10^{-6})} \tag{22}$$

$$\frac{\tilde{v}_{\rm out}}{\tilde{v}_{\rm in}} = \frac{12.264}{1+s\,(553.3\times10^{-6})}. \tag{23}$$

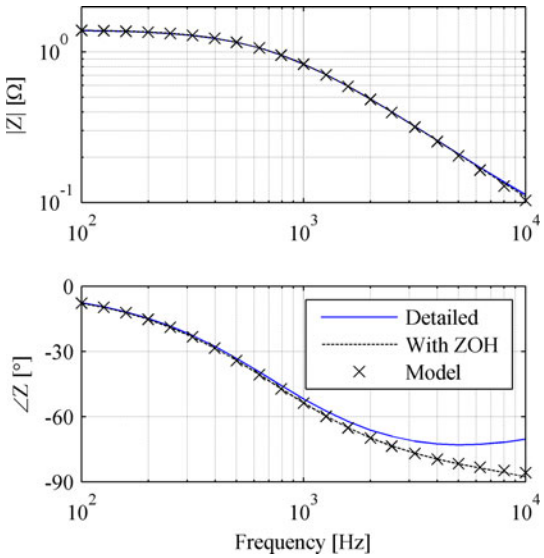

Fig. 6. Output impedance from detailed simulation and reduced-order model of the three-stage Fibonacci. "With ZOH" implies the use of zero-order holds around the simulated perturbation and measurement.

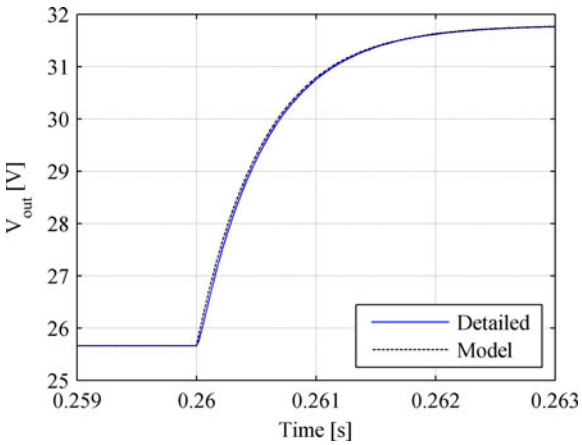

Fig. 7. Detailed simulation and model response to step in $v_{\rm in}$ (2.0 to 2.5 V), five stage.

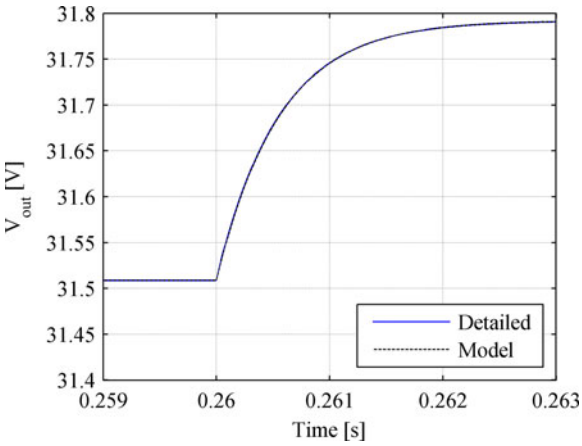

Fig. 8. Detailed simulation and model response to step in $v_{\rm th}$ (15 to 20 V), five stage.

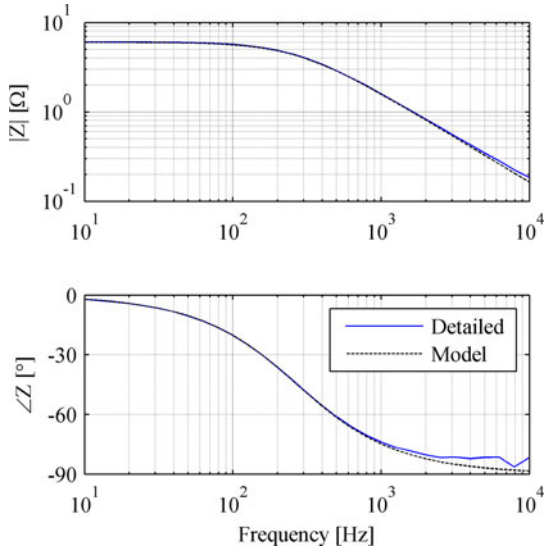

Fig. 9. Output impedance of the five-stage Fibonacci converter, comparing simulation to the derived model.

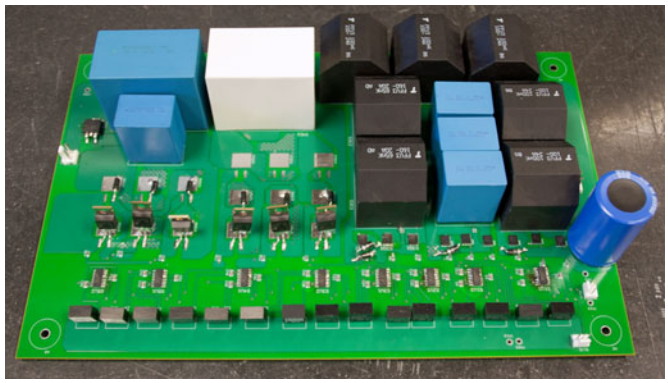

Fig. 10. Five-stage Fibonacci converter.

The lower cutoff frequency of this converter, as compared to the previously analyzed three-stage converter, masks the zero-order-hold effect over the frequency range of interest.

The advantage of the proposed method is that the model can be used to quickly generate dynamic models of an SC converter of a particular topology. A MATLAB (or equivalent) program may be written with the matrices corresponding to Table I, with resistances, capacitances, and switching parameters left as variables. As components and switching parameters are varied, these matrices may be used to sweep first the static characteristic (as in [13]) to ensure proper steady-state performance, and then the dynamic characteristics (as in Figs. 4–9) to ensure proper dynamic characteristics. This is a much more efficient process than simulating each candidate design.

V. Experimental Fibonacci Converter

An experimental five-stage Fibonacci converter was constructed for further validation. A photograph of the converter is shown in Fig. 10. In a practical Fibonacci converter, the different voltage on each stage necessitates different MOSFETs

TABLE II
STAGE COMPONENTS FOR FIVE-STAGE FIBONACCI CONVERTER

Stage	Capacitor	Switch
Stage 1	5x FFV34E0107K – 100 µF Film	SIR870ADP-T1-GE3 N-CH100V 63A
Stage 2	3x B32524Q1686K – 68 µF Film	SIR870ADP-T1-GE3 N-CH 100V 63A
Stage 3	2x FFV34F0656K – 65 µF Film	BSC320N20NS3 N-CH 200V 36A
Stage 4	1x C4ATDBW5600A30J – 60 µF Film	SIHP22N60S-E3 N-CH 600V 22A
Stage 5	1x B32774D4226K – 22 µF Film	SIHP22N60S-E3 N-CH 600V 22A
Stage 6	1x B32798G2756K – 75 µF Film	C3D10060G SiC Schottky 600V 10A

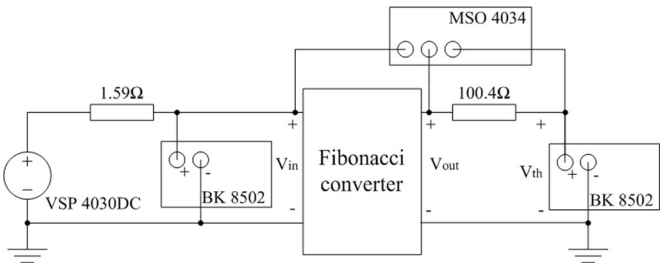

Fig. 11. Experimental set-up.

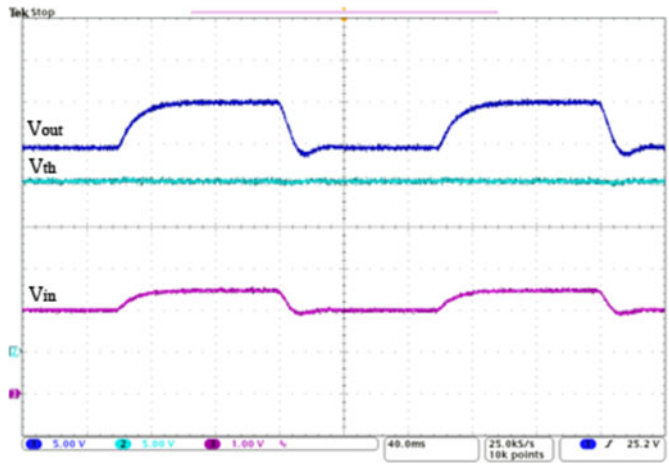

Fig. 12. Response to a square-wave input voltage disturbance.

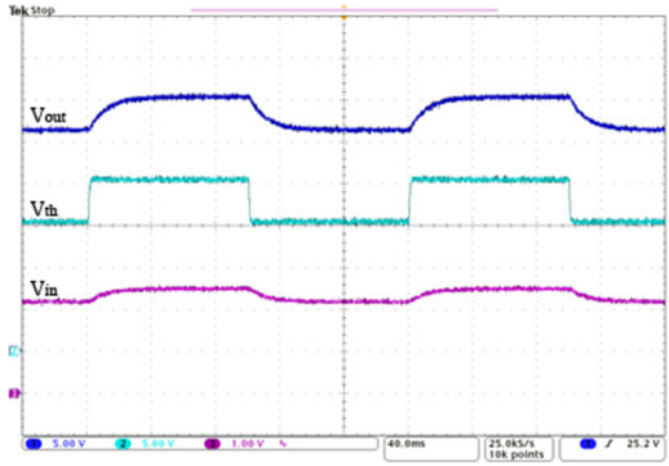

Fig. 13. Response to a square-wave Thevenin voltage disturbance.

and capacitors. Table II lists the component selections for each stage. Electrolytic capacitors have relatively high inductance and resistance that combine to limit converter performance, and also have known reliability problems [24]. These problems are well known and have led to sophisticated models and innovative converter topologies in applications such as solar microinverters and off-line LED drivers [25]–[27]. Therefore, in this study, film capacitors were used for all switching stages.

The prototype converter was operated with a switching frequency fixed at 50 kHz and a duty cycle of 45%. As in any power converter, switching frequency is a design tradeoff. For more discussion, see [13] and [14]. The converter, as designed, is effective up to approximately 100 kHz, beyond which stray inductance degrades performance. At 50 kHz, performance is adequate and gate-drive power is reasonable. The converter was powered by a BK Precision VSP 4030 dc power supply. To create the required disturbance in input voltage a BK Precision 8502 electronic load in transient voltage mode was put in parallel to the converter input. A 10 W, 1.59 -Ω resistor was inserted between the dc source and the electronic load as a current limiter. A 10 W, 100.4-Ω resistor in series with a BK Precision 8502 electronic load in transient voltage mode was connected to the output of the converter as a Thevenin load. A Tektronix MSO 4034 oscilloscope was used to measure the I/O of the converter and the Thevenin voltage of the electric load. The experimental setup is shown in Fig. 11. In Figs. 12 and 13, the top trace is the output voltage of the converter, the middle plot is the Thevenin voltage portion of the load, and the bottom trace is the input voltage.

With the Thevenin voltage fixed at 20 V, the converter was subjected to a square-wave input voltage disturbance varying between 2 and 2.5 V. Fig. 12 shows the response of the converter to the input disturbance. With the input voltage fixed at 2.5 V, the converter was subjected to square-wave Thevenin voltage disturbance varying between 15 and 20 V. Fig. 13 shows

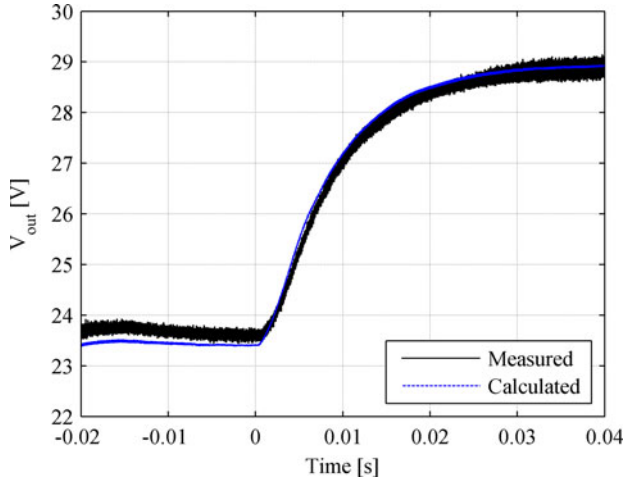

Fig. 14. Response to a positive input voltage step (2.0 to 2.5 V).

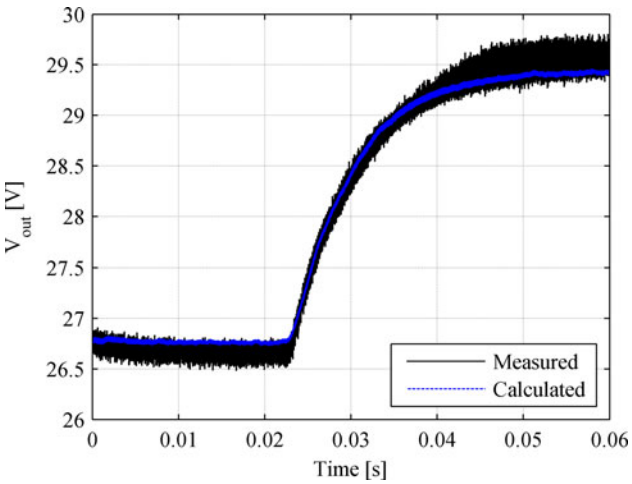

Fig. 15. Response to a positive Thevenin voltage step (15 to 20 V).

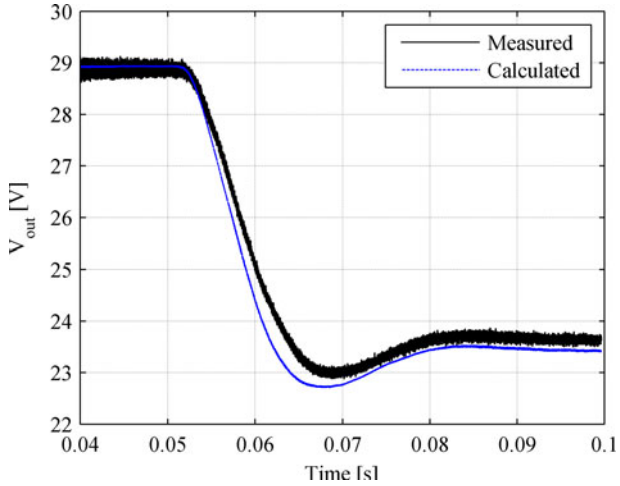

Fig. 16. Response to a negative input voltage step (2.5 to 2.0 V).

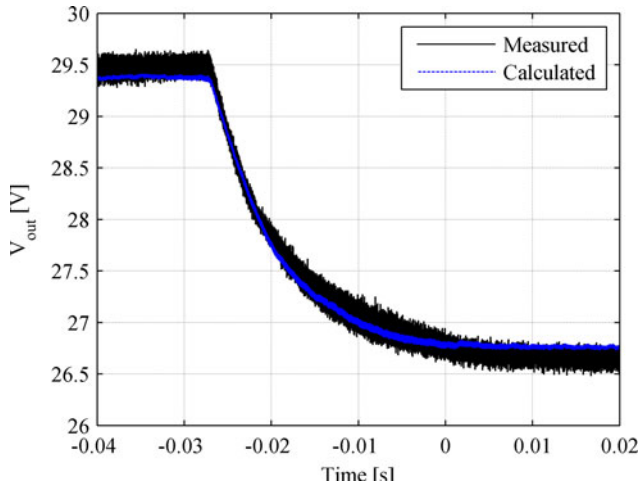

Fig. 17. Response to a negative Thevenin voltage step (20 to 15 V).

the response of the converter to the load disturbance. The input voltage changes slightly during the load disturbance due to source and wiring impedance.

The measurements from the disturbance tests were used to verify the accuracy of the proposed reduced-order model. The measurements taken with the MSO4034 oscilloscope were exported as data points to a computer for processing. The data points corresponding to Figs. 12 and 13 were imported into MATLAB and used as the input to the simplified model from the preceding section, using `lsim`. This was done in order to compare the model's prediction to the actual converter behavior under the same operating conditions. The predicted disturbance responses and the measured responses were superimposed onto one another to evaluate the accuracy of the reduced-order model. Figs. 14–17 compare the model prediction and the behavior of the experimental converter subjected to the different types of disturbances. The small difference seen in Fig. 16 most likely results from parasitic inductances that have been neglected here or from errors in resistance measurements. The undershoot, which is not expected in a first-order system, is an appropriate response to the undershoot of the electronic load connected to the input terminals.

VI. Conclusion

A reduced-order dynamic model of an SC converter was derived from the differential equations that describe the circuit in each mode. Most practical SC converters may be modeled as first-order systems with two inputs and corresponding dc gains. The dc gains of the full-order system and its dominant eigenvalue in the discrete-time domain were used to create the reduced-order model in the Laplace domain. The model was validated with simulations and experiments. The model matches both detailed switching simulations and practical experimental converters. Designers may use this model to ensure that an SC converter meets load and input transient specifications in sensitive applications. Dynamic performance is important for ac–ac topologies such as in [28]. Also, in systems that require further power conversion for precise voltage regulation, the modeled output impedance may be used to verify system stability according to known criteria, such as the Middlebrook impedance

matching requirement [29]. In a typical application, an SC converter as shown here would be used to provide a fixed gain like a transformer, and another converter (e.g., buck or boost) would be used to provide precise regulation. For example, a system might have a relatively high distribution voltage, e.g., 48 V, stepped down to a relatively low but unregulated voltage like 12 V with an SC converter, and precisely regulated with a buck converter to service a 3.3-V or lower microprocessor load. With knowledge of the SC converter's dynamics and impedance characteristics, the complete system may be designed to meet end-to-end dynamic specifications.

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