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An On-line Fault Location Technique for DC Microgrid Using Transient Measurements

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***Abstract*—Locating faults in meshed dc microgrids poses challenges due to low impedance offered by the dc network. In this paper, an on-line fault location scheme which can be implemented as an additional feature in a relay is proposed. The algorithm is developed to determine fault location based on voltage and current transients. Both line to line and monopole ground faults are analysed separately and algorithms are developed based on the rate of change of current. Direct short circuit faults are located using transient measurements captured locally, while communication based technique is utilized to locate the impedance faults. The developed fault location technique is also capable of estimating the fault resistance accurately. The algorithm is validated on a ± 600 V meshed dc grid, for both the types of faults under wide range of fault impedance at different fault locations.**

***Index Terms*—Current measurement, dc microgrid, fault location, fault transient, voltage measurement.**

I. Introduction

In recent past, significant research and development efforts have been made to integrate renewable energy sources, such as wind turbines, and photovoltaic systems into the power distribution networks [1], [2]. Along with this, the development in power electronics had made easy integration of the renewable sources posssible with dc grids. Key advantage of a dc microgrid as compared to an ac microgrid is that loads, sources, and energy storage are connected through simpler and more efficient power-electronic interfaces [3]. Other advantages include its higher efficiency [4], ease of paralleling of sources on dc bus [5], and more power transfer capacity [6]. However, fault detection, arc breaking, dc switchgear and unavailability of standards, guidelines and experience are the major issues in the dc network protection [3], [5].

Ability to accurately locate a fault in a microgrid leads to many advantages, such as quick maintenance, fast restoration, and, hence, reduction in power outage duration. Primitive methods of fault location include time consuming visual inspection [7]. Automatic fault location methods are most widely used, which are based on determining the physical location of the fault by processing the voltage and current measurements. A fault location function can be implemented into protective relay, digital fault recorder or a stand alone fault locator [8]–[14]. Available literature on fault location techniques for dc distribution systems is broadly categorized as:

Off-Line Methods: In this category, the fault in dc cable can be located after isolating the faulty section from the healthy network using an external device called fault locator or Power Probe Unit (PPU). PPU may consist of active [9] or passive [8], [10] electrical components. The signal is injected into the isolated cable using the PPU and is analysed using different schemes, such as least square based non-iterative method [8], voltage divider [15], and equivalent impedance based methods [9]. To locate the fault automatically, a PPU is required to be connected at each cable section. This may increase the overall cost. Even for the portable PPUs [8], human intervention may be required, thereby, adding to the cost. Moreover, these methods are not designed for online applications because PPU is required to be connected on the de-energised network.

On-Line Methods: Under this category, the fault location algorithm is in-built in the protection relays. Some of the methods implemented to locate the fault include Wavelet Transform (WT) based Multi-Resolution Analysis (MRA) [16], Artificial Neural Network (ANN) based methods [11], [12], and methods based on travelling wave approach. The travelling wave based methods utilize the fact that a wave is generated from the fault point and propagates along the conductors [13], [14]. The distance could be calculated by detecting the time taken by the travelling wave to propagate from the fault point to the measuring point. However, its accuracy is easily influenced by the factors, such as measurement of travel time, propagation velocity, high sampling frequency, and interference signals [17]. It is difficult to distinguish various types of wave heads in a microgrid due to the short length of the feeders.

Both line to line and line to ground fault location techniques for low voltage dc microgrid are discussed in reference [15], [18] using parameter estimation approach. In these methods the voltage and current transients are captured and processed locally to estimate the fault location in terms of the cable parameters. In reference [15], the system information such as converter filter capacitor value is required to accurately estimate the fault location. Reference [18] validated the method for radial dc network, which may not give accurate result for the meshed dc system with bidirectional power flow. The fault location in dc network highly depends upon fault resistance and its architecture and requires data from both the ends to accurately locate the fault.

The concept of smart grid and microgrid requires sensors and communication networks to be provided in order to monitor the system condition and avoid outages. The available communication infrastructure is utilized to locate the fault in the dc microgrid. In this paper, a protection scheme for the smart dc microgrids with ring configuration is proposed. The line parameters upto the fault point are estimated using the voltage and the current data measured by the protective device

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(PD) connected at both the ends of the cable. Along with this, the fault resistance is also determined using the fault location information. Issues related to the communication, such as data synchronization, time delay, are also discussed in this paper.

The paper is organised as follows. In Section II, the dc microgrid architecture taken as the test system, its components and ratings are explained in brief. The fault current in analysed and the proposed fault location algorithm is discussed in Section III. In Section IV, the issues in implementing the proposed algorithm are discussed in details. The numerical simulation based validation is performed and the results are discussed in section V. Conclusions are provided in section VI.

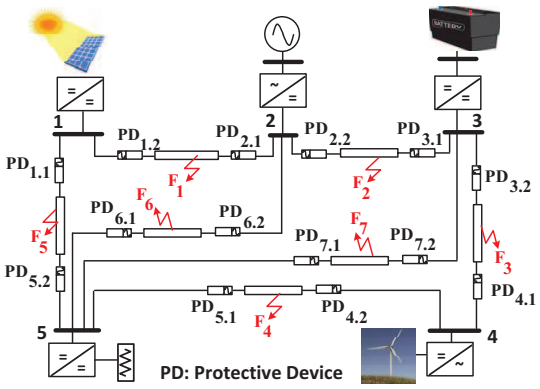


Fig. 1. DC microgrid test system

II. Test System

A ring type Low Voltage dc (LVdc) microgrid, as shown in Fig. 1, has been simulated in Real Time Digital Simulator (RTDS). The two level Voltage Source Converters (VSCs) are utilized to interface the dc grid with the renewable sources and the ac grid, whereas dc/dc converters are used for integrating battery and solar PV system. Other design factors such as converter components values, its control parameters are explained in [19]. The operating dc voltage of the grid is ± 600 V pole to ground. The component ratings of all the modules are given in Table I.

TABLE I
Rating of dc Microgrid Components [19]

System Component	Rating
DC Grid Voltage	± 600 V
Battery dc-dc Converter	$0.5MW$
Battery	$300V$, $1.3kAh$, Nickel Cadmium
PV Converter	$0.5MW$
Solar Panel	$V_{mp} = 54.7V$, $I_{mp} = 5.58A$ at STC
Grid VSC	$1MW$
Wind Turbine	$1MW$, PMSG
Cable Resistance r_{pu}	$10m\Omega$/km
Cable Inductance L_{pu}	$100\mu H$/km
Filter Capacitor, C	$25mF$
Load	Constant impedance load 500 kW

Various international standards generally recommend TN-S grounding scheme for the dc system [20], wherein the positive and negative poles are at equal potential difference with respect to ground. The benefit of this type of grounding is that the load remains energised even if one pole is under fault, provided that there is no source that trips due to over voltage [21]. This situation makes the fault detection and location even more difficult. From protection design point of view, the grid is equipped with 10 PDs, placed on both the sides of the dc cables. To represent each pole distinctly, superscript p is used to denote positive pole and n for negative pole. Faults $F_1 - F_7$ represent either LL or LG faults. The current direction of all PDs is assumed as positive towards the cable. Subscript of LL and LG are used to differentiate between both types of faults.

III. Cable Fault Analysis

Mainly two types of network faults occur in dc network i.e., pole to pole and pole to ground. Out of two, pole-to-ground fault occurrence is very frequent. It mat be due to the physical damage, ageing or severe electrical stress in the cables during operation. The two type of faults are analysed separately in the following sections to derive the conditions for fault location.

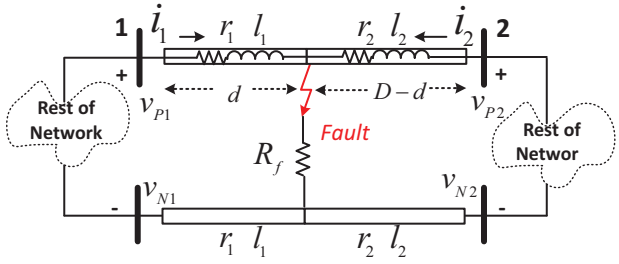


Fig. 2. System network for line to line fault

A. Line to Line Fault

A line to line fault is considered possible in any of the cable section of system shown in Fig. 1. The faulted network viewed from the PDs' side connected on the both sides of the cable is shown in Fig. 2. As the fault occurs the cable current seen by the PD increases, and the voltage during fault transient can be written as,

$$2l_1 \frac{di_1}{dt} = v_1 - 2i_1 r_1 - (i_1 + i_2)R_f \quad (1)$$

$$2l_2 \frac{di_2}{dt} = v_2 - 2i_2 r_2 - (i_1 + i_2)R_f \quad (2)$$

where, v_1, v_2 are the line to line voltage at terminal 1 and 2, respectively, and can be written as $v_1 = v_{P1} + v_{N1}$, and $v_2 = v_{P2} + v_{N2}$. Values l_1, r_1 and l_2, r_2 are the equivalent cable parameters upto the fault point seen by the respective terminals. The cable parameters can also be written as,

$$l_1 = (d)L_{pu}, \qquad r_1 = (d)R_{pu} \quad (3)$$

$$l_2 = (D-d)L_{pu}, \qquad r_2 = (D-d)R_{pu} \quad (4)$$

where, d is the distance of the fault from terminal 1 and D is total length of the cable. It is also noticed that l_1/r_1 ratio remains constant even under the fault transient [8], and is written as,

$$\frac{R_{pu}}{L_{pu}} = \frac{r_1}{l_1} = \frac{R}{L} = 2\alpha \quad (5)$$

where, $\{R, L\}$ is the total resistance, inductance of the cable, which can be calculated as $\{R_{pu}, L_{pu}\}$ times the total length of the cable (D).

To make the fault location algorithm independent of the fault resistance, subtract (2) from (1). The difference in the transient voltage across the inductors at the two ends will be equal to their bus voltage difference and voltage drop in the cable and is independent of the fault resistance. Using (1)-(5), the fault distance d is calculated as,

$$d = \frac{v_2 - v_1 + Ldi_2/dt + i_2 2\alpha L}{(di_1/dt + di_2/dt + 2\alpha(i_1 + i_2))L_{pu}} \tag{6}$$

Using the fault location information, the fault resistance is determined. Since the distributed cable model is assumed for the fault analysis, once the fault location is identified, the cable parameter upto the fault point is calculated using (3) and (5). The fault resistance R_f is written as,

$$R_f = \frac{v_1 - dL_{pu}di_1/dt - dR_{pu}i_1}{i_1 + i_2} \tag{7}$$

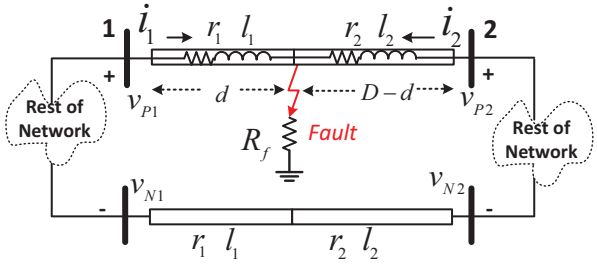


Fig. 3. System network for monopole ground fault

B. Line to Ground Fault

A similar expression is derived for the LG fault in the network as shown in Fig. 3. The transient measurements are captured on both the sides and utilized to locate the fault. The transient voltage for the positive pole to ground fault can be written as,

$$l_1\frac{di_1}{dt} = v_{P1} - i_1r_1 - (i_1 + i_2)R_f \tag{8}$$

$$l_2\frac{di_2}{dt} = v_{P2} - i_2r_2 - (i_1 + i_2)R_f \tag{9}$$

where, (v_{P1}, v_{P2}) are the positive pole to ground voltage measured by the PDs connected at terminals 1 and 2, respectively. Using (3)-(5) and (8)-(9), the expression for the LG fault is written as,

$$d = \frac{v_{P2} - v_{P1} + Ldi_2/dt + i_2\alpha L}{(di_1/dt + di_2/dt + \alpha(i_1 + i_2))L_{pu}} \tag{10}$$

Using the fault location information from (10), the fault resistance can be determined as,

$$R_f = \frac{v_{CP1} - dL_{pu}di_1/dt - dR_{pu}i_1}{i_1 + i_2} \tag{11}$$

In case of the bolted LL and LG faults the term $(i_1+i_2)R_f$ is considered as very low as compared to the other terms and hence, neglected. Since the bolted faults are the most severe faults and are time critical, therefore it needs to be located as soon as possible. Because of this, the bolted faults are located by utilizing only the local measurements in the following equations for LL and LG faults.

$$d = \begin{cases} \frac{v_1}{2L_{pu}(di_1/dt + \alpha i_1)} & \text{LL Fault} \\ \\ \frac{v_{P1}}{L_{pu}(di_1/dt + \alpha i_1)} & \text{LG Fault} \end{cases} \tag{12}$$

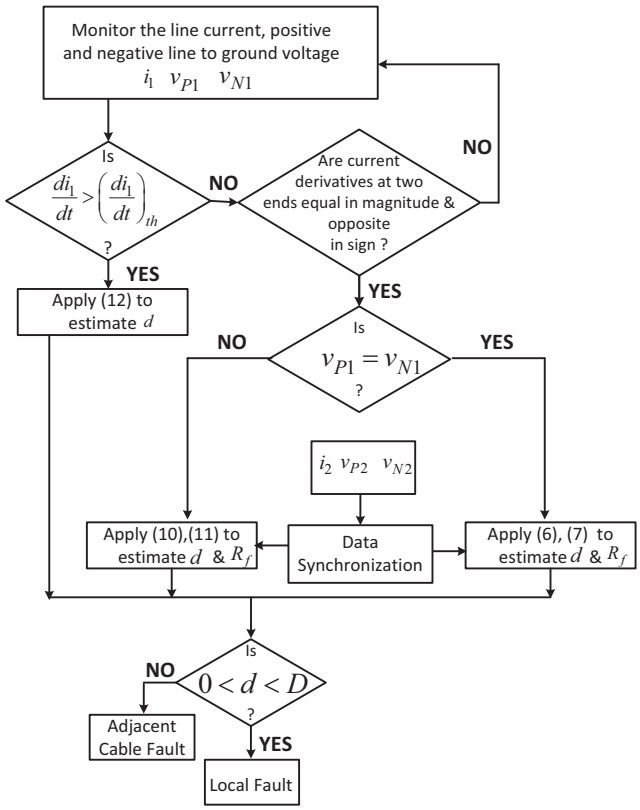


Fig. 4. Proposed fault location algorithm

C. Proposed Algorithm

Two types of faults, LL and LG, can be differentiated by monitoring the dc link voltage (v) and individual pole to ground voltage (v_{P1}, v_{N1}) at each line terminal. During normal operation and LL fault, the monopole voltage, v_{P1} and v_{N1} remain equal and add upto total dc voltage, v. On the other hand, the difference between the two voltages indicate monopole ground fault. Short circuit faults are associated with high di/dt. As the measured di/dt exceeds the threshold, it enters into fault location subroutine, which utilizes local measurements. The threshold for the short circuit fault is calculated as [22],

$$\left(\frac{di}{dt}\right)_{th} = \frac{v_{P1}(0)}{L} = \frac{v_{N1}(0)}{L} = \frac{v_{P1}(0) + v_{N1}(0)}{2L} \tag{13}$$

where, L is the inductance of the full length cable. For impedance faults, the measured di/dt at the two ends will be equal and of opposite sign. Hence, it calls for the communication based algorithm. The data collected from the other

terminal is processed for time synchronization (discussed in following section) and, then, utilized to locate the fault, as shown in Fig. 4. The calculated cable inductance upto the fault point indicate the fault location. If the calculated cable length d is more than the total cable length D, the fault occurs in the adjacent cable.

IV. Implementation Requirements

There are mainly two key requirements to implement the proposed fault location technique for the dc microgrids. These are,

1. Fault location within desirable duration
2. Synchronization of data measured at two ends of the cable during a fault

A. Desirable Duration for Fault Location

Direct short circuit faults are more severe than the impedance faults and need to be located within the critical time [22], [23]. The overall time available to locate the fault (t_{fl}) in the dc network is written as,

$$t_{fl} = t_{cr} - t_{cb} - t_{misc} \tag{14}$$

where, t_{cr} is the critical time, typically 2 ms determined by the converter and associated components in the dc microgrid [24], [25]. t_{cb} is the circuit breaker operating time, typical 500 μs for hybrid and solid state CB [26], [27]. Other miscellaneous delay t_{misc} includes communication delay associated with the data transfer. To avoid the communication delay and other issues related to the communication, such as data synchronisation, local measurement based fault location technique is employed. The technique is applied for short circuit faults, which are time critical. For impedance faults, t_{cr} is much more than 2 ms and depends upon the fault resistance and the microgrid architecture. Hence, the faults can be accurately located using communication based two end measurements.

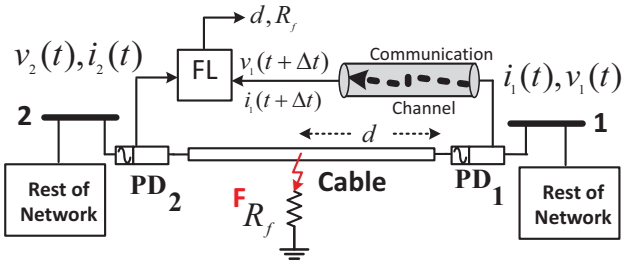


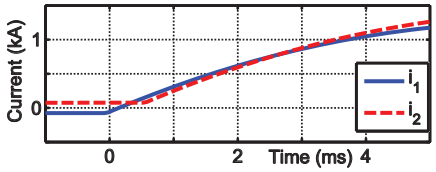
Fig. 5. Proposed fault location algorithm

B. Data Synchronization

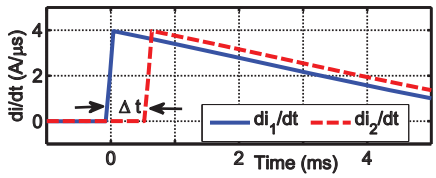
In case of impedance faults the voltage and current are measured at the two ends of cable and communicated at other end to locate the fault as shown in Fig. 5. Mathematical expressions (6)-(7) and (10)-(11) are not applicable directly on the measured data to locate the fault. It is required to synchronize the two measurements to locate the fault accurately. In traditional ac systems mainly two methods are utilized to synchronize the data with time [7]:

1. Determining the time relation between pre-fault quantities
2. Time synchronization using fault measurements

Traditional fault location methods in ac systems utilized pre fault measurements to calculate the synchronization angle and compensated for the delay in the measurements at the two ends of the cable. But it can not be utilized in the dc power system due to the absence of the phasor quantities.



(a)



(b)

Fig. 6. Unsynchronized (a) current measurements and, (b) its derivatives observed at one terminal

In ac networks, the boundary condition of the faults, such as positive sequence components in case of balanced three phase faults, are utilized to synchronized data at two ends. Similar approach has been adopted to synchronize the measurements at the two ends of cable for dc microgrid. A fault in the dc network results in high di/dt, which is utilized as the boundary condition for synchronization. The time stamped voltage and current measurements at the remote end are sampled using Intelligent Electronics Device (IED). The sampled data is communicated to the other end with the time delay of Δt, as shown in Fig. 6a. The rate of change of line current is computed for both the currents and compared to get the time delay, as shown in Fig. 6b.

V. Validation of the Proposed Method

To validate the proposed fault location algorithm, it is tested on a loop architecture of a dc microgrid, as shown in Fig. 1. The proposed algorithm to locate the fault on-line using the transient response during fault has been validated using Real Time Digital Simulator (RTDS).

A. Short Circuit Faults

The LL and LG faults at F_5 are simulated, at a distance of 1 km from $PD_{1.1}$. The data sampled by the digital relay during the fault is utilized to determine the location. The sampling rate is chosen as 50 μs decided based on the transient time of the fault current. The measurements are assumed to be captured during the fault by the digital relay of $PD_{1.1}$, as shown in Fig. 7. The algorithm is initiated when the di/dt exceeds its threshold and continues for consecutive next 5 samples .

The data at the relay terminal such as voltage, current, and its derivatives are sampled. All the measurements are

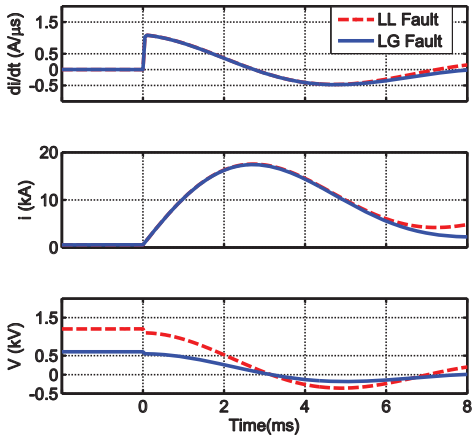


Fig. 7. Voltage and current transients captured by $PD^p_{1.1}$ during the LL and LG fault, F_5

TABLE II
DATA STORED BY $PD^p_{1.1}$ DURING BOLTED FAULT TRANSIENT

v_{P1} (kV)	i_1 (kA)	di_1/dt (A/μs)	d (m)	v_1 (kV)	i_1 (kA)	di_1/dt (A/μs)	d (m)
0.602	0.55	0.00	-	1.203	0.54	0.00	-
0.549	1.06	10.66	1.017	1.097	1.06	10.69	1.016
0.548	1.61	10.84	0.997	1.096	1.60	10.84	0.996
0.547	2.14	10.76	0.997	1.095	2.14	10.76	0.998
0.546	2.68	10.67	0.998	1.091	2.67	10.68	0.997
0.541	3.21	10.58	0.992	1.087	3.20	10.59	0.997

utilized to estimate the fault location, as given in Table II. The location is calculated for individual set of data using (12). The calculated distance is averaged over five samples to avoid any measurement noise error. This has provided the estimation of 1.0002 km for the LG and 1.0008 km for the LL faults from $PD_{1.1}$. It can be noticed that the fault is located with 5 sample intervals and, hence, the voltage (v_{LL} or v_{LG}) does not drop below the limit where free-wheeling diode starts conducting.

TABLE III
LL AND LG BOLTED FAULTS AT DIFFERENT LOCATIONS IN FIG. 1

Fault F_x	$PD_{x.2}$	**Fault distance** d **(m)**	**Estimated** d**(m)**	**Error (m)**	**Error** (ϵ_d) **(%)**
F_{2LL}	$PD_{2.2}$	240	240.5	0.5	0.21
F_{3LL}	$PD_{3.2}$	60	59.9	0.1	0.17
F_{4LL}	$PD_{4.2}$	900	900.5	0.5	0.05
F_{1LL}	$PD_{1.2}$	850	849.8	0.2	0.011
F_{6LL}	$PD_{6.2}$	50	49.5	0.5	1
F_{7LL}	$PD_{7.2}$	107	106.6	0.4	0.37
F_{1LG}	$PD_{1.2}$	300	299.5	0.5	0.17
F_{2LG}	$PD_{2.2}$	165	164.5	0.5	0.3
F_{3LG}	$PD_{3.2}$	160	160.2	0.2	0.12
F_{4LG}	$PD_{4.2}$	570	569.8	0.2	0.03
F_{6LG}	$PD_{6.2}$	550	449.9	0.1	0.02
F_{7LG}	$PD_{7.2}$	100	99.6	0.4	0.4
F_{4LL}	$PD_{4.2}$	220	219.5	0.5	0.23
F_{1LG}	$PD_{2.2}$	270	269.6	0.4	0.15
F_{3LL}	$PD_{3.2}$	196	195.5	0.5	0.255
F_{2LG}	$PD_{1.2}$	990	989.6	0.4	0.04

The faults $\{F_1, F_2, ...F_7\}$ are simulated at distance d_L, d_G from their respective $PD_{x.2}$ where, $x\epsilon\{1, 2, ..., 7\}$ are the line numbers. Both LL and LG faults are simulated at different locations and the results are given in Table III. The percentage error in the fault location is computed as,

$$\epsilon_d(\%) = \frac{|d_{act} - d_{cal}|}{d_{act}} \times 100\% \quad (15)$$

where, d_{act} is the actual fault distance and d_{cal} is the fault distance calculated using the proposed algorithm. It is found that the faults are accurately located within 5 sample intervals, which is much smaller than t_{pk}.

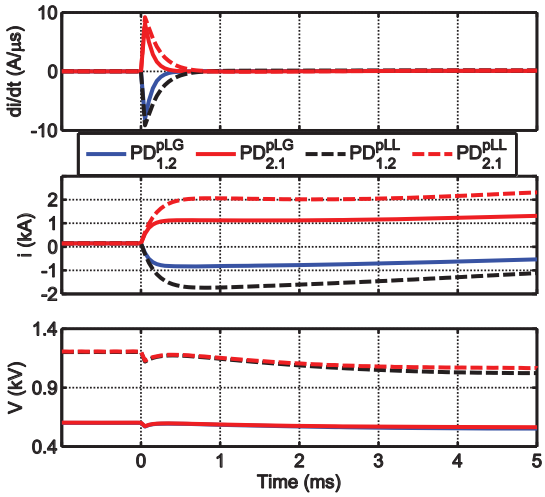


Fig. 8. Fault transients captured by $PD^p_{1.2}$ and $PD^p_{2.1}$ during the LL and LG fault F_1 with 0.3 Ω fault resistance

B. Impedance Fault

The LG fault F_1 is simulated at a distance of 500 m from the $PD^p_{1.2}$ with fault resistance of 0.3Ω. The data stored by $PD^p_{1.2}$ and $PD^p_{2.1}$ during the fault, as given in Table IV, and the transients are shown in Fig. 8. The fault location and resistance are calculated for the individual measurement set and the average distance and fault resistance are found as 500 m and 0.303 Ω, respectively.

TABLE IV
DATA STORED BY $PD^p_{1.2}$ AND $PD^p_{2.1}$ DURING LG FAULT WITH FAULT RESISTANCE OF 0.3Ω

$PD_{1.2}$ Data			$PD_{2.1}$ Data			Estimated	
v_1 (kV)	i_1 (kA)	di_1/dt (A/μs)	v_2 (kV)	i_2 (kA)	di_2/dt (A/μs)	d (km)	R_f (Ω)
0.601	0.15	0.00	0.603	0.15	0.00	-	-
0.580	0.41	8.12	0.573	0.70	8.15	0.510	0.33
0.583	0.66	4.98	0.585	0.80	5.01	0.496	0.31
0.590	0.80	2.85	0.592	0.95	2.88	0.495	0.30
0.593	0.88	1.63	0.595	1.03	1.64	0.493	0.29
0.597	0.93	0.92	0.596	1.07	0.93	0.506	0.28

Similar calculations have been done for the LL fault at the same location, which results into the distance estimation of 499.8 m and resistance of 0.301Ω. Faults with different impedances and locations on the dc system, shown in Fig. 1, are simulated and % error in the location, is given in Table V.

With the maximum fault resistance of 1Ω [8], [28], the voltage and current transients damped out quickly. Hence, the number of samples to locate the fault reduces as the fault distance increases, and % error in locating the fault increases. However, the maximum absolute error in fault resistance is found not more that 350 mΩ.

TABLE V
PERCENTAGE ERROR IN LL FAULT F_5 LOCATION FOR DIFFERENT R_f

Fault Location	**Fault Resistance** R_f (Ω)				
d(%)	0.2	0.4	0.6	0.8	1
20	23	28	25	32	35
40	12	21	23	22	25
50	15	18	21	29	31
60	13	15	16	25	28
80	11	13	15	18	21
100	8	11	13	20	25

VI. CONCLUSION

For accurately locating a fault and determining the fault resistance in a dc microgrid, a new approach has been proposed in this paper. Two types of faults, i.e., LL and LG, have been identified using the voltage measurements and studied under various fault resistances. Based on their transient characteristics, the faults have been further classified as bolted fault and impedance fault. In the direct short circuits, the current transients depend upon the fault location and may lead to system voltage collapse. The time to locate such faults is very critical, which are located within 0.25 ms after the fault inception using the local measurements.

On the other hand, the impedance fault transients highly depend upon the fault resistance and its location. As a result, the measurements at the two ends are required to locate such faults. The data measured at the two ends are synchronized before applying the algorithm. The accuracy of the proposed method has been successfully tested for different fault locations and fault resistance values ranging from few milli-Ω to Ωs.

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REFERENCES

[1] R. Dugan and T. McDermott, "Distributed generation," *IEEE Ind. Appl. Mag.*, vol. 8, no. 2, pp. 19–25, Mar./Apr. 2002.

[2] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1398–1407, Oct. 2006.

[3] D. Salomonsson and A. Sannino, "Low-voltage dc distribution system for commercial power systems with sensitive electronic loads," *IEEE Trans. Power Del.*, vol. 22, no. 3, pp. 1620–1627, July 2007.

[4] M. Starke, L. Tolbert, and B. Ozpineci, "AC vs. DC distribution: A loss comparison," in *Proc. IEEE/PES Transmission Distribustion Conference Exposition*, 2008, pp. 1–7.

[5] D. Salomonsson, L. Soder, and A. Sannino, "Protection of low-voltage DC microgrids," *IEEE Trans. Power Del.*, vol. 24, no. 3, pp. 1045–1053, July 2009.

[6] M. Starke, L. Fangxing, L. M. Tolbert, and B. Ozpineci, "AC vs. DC distribution: Maximum power transfer capability," in *Proc. IEEE/PES Conversion Delivery Electrctical Energy 21st Century*, 2008, pp. 1–6.

[7] M. M. Saha, J. Izykowski, and E. Rosolowski, *Fault Location on power networks*. Springer-Verlag London, 2010.

[8] R. Mohanty, U. S. M. Balaji, and A. K. Pradhan, "An accurate non-iterative fault-location technique for low-voltage DC microgrid," *IEEE Trans. Power Del.*, vol. 31, no. 2, pp. 475–481, 2016.

[9] E. Christopher, M. Sumner, D. Thomas, W. Xiaohui, and de Wildt, "Fault location in a zonal DC marine power system using active impedance estimation," *IEEE Trans. Appl. Ind.*, vol. 49, no. 2, pp. 860–865, 2013.

[10] M. M. Xu, L. Y. Xiao, and H. F. Wang, "A prony-based method of locating short-circuit fault in DC distribution system," in *Renewable Power Generation Conference, 2nd IET*, 2013, pp. 1–4.

[11] C. Chang, S. Kumar, B. Liu, and A. Khambadkone, "Real-time detection using wavelet transform and neural network of short-circuit faults within a train in dc transit systems," in *IEE Proceedings Electric Power Applications*, vol. 128, May 2001, pp. 251–256.

[12] N. Chanda and F. Yong, "Ann-based fault classification and location in mvdc shipboard power systems," in *North American Power Symposium, Boston*, Aug. 2011, pp. 1–7.

[13] O. M. K. K. Nanayakkara, A. D.Rajapakse, and R. Wachal, "Traveling-wave-based line fault location in star-connected multiterminal HVDC systems," *IEEE Trans. Power Del.*, vol. 27, no. 4, pp. 2286–2294, July 2012.

[14] S.Azizi, M. Pasand, M.Abedini, and A.Hassani, "A traveling wave-based methodology for wide area fault location in multiterminal DC systems," *IEEE Trans. Power Del.*, vol. 29, no. 6, p. 25522560, Dec. 2014.

[15] J. Yang, J. E. Fletcher, and J. OReilly, "Short-circuit and ground fault analyses and location in vsc-based dc network cables," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3827–3837, Oct 2012.

[16] L. Weilin, L. Min, A. Monti, and F. Ponci, "Wavelet based method for fault detection in medium voltage dc shipboard power systems," in *IEEE International Instrumentation and Measurement Technology Conference*, 2012, pp. 2155–2160.

[17] J. Suonan, S. Gao, G. Song, Z. Jiao, and X. Kang, "A novel fault location method for HVDC transmission lines," *IEEE Trans. Power Del.*, vol. 25, pp. 1203–1209, 2010.

[18] X. Feng *et al.*, "Fault inductance based protection for dc distribution systems," in *Proc. of the 13th International Conference on Developments in Power System Protection, Edinburgh, Scotland*, 2016, pp. 1–6.

[19] L. Xu and D. Chen, "Control and operation of DC microgrid with variable generation and energy storage," *IEEE Trans. Power Del.*, vol. 26, no. 4, pp. 2513–2521, 2011.

[20] B. Jover. Choosing the right earthing system, schneider electric: Energy regulations. [Online]. Available: http://blog.schneider-electric.com/energy-regulations/2014/01/03/choosing-right-earthing-system/

[21] Y. Wang *et al.*, "Performance of shipboard medium-voltage dc system of various grounding modes under monopole ground fault," *IEEE Trans. Ind. Appl.*, vol. 51, no. 6, pp. 5002–5009, 2015.

[22] A. Meghwani, S. Srivastava, and S. Chakrabarti, "A non-unit protection scheme for dc microgrid based on local measurements," *IEEE Trans. Power Del.*, vol. 32, no. 1, pp. 172–181, 2017.

[23] J. D. Park, J. Candelaria, L. Ma, and K. Dunn, "DC ring-bus microgrid fault protection and identification of fault location," *IEEE Trans. Power Del.*, vol. 28, no. 4, pp. 2574–2584, 2013.

[24] S. D. A. Fletcher, P. J. Norman, S. J. Galloway, P. Crolla, and G. M. Burt, "Determination of protection system requirements for DC unmanned aerial vehicle electrical power network for enhance capability and survivability," in *Proc. IET Electrical Systems in Transportation*, vol. 1, July 2011, pp. 137–147.

[25] S. D. A. Fletcher, S. J. Galloway, P. J. Norman, P. Crolla, and G. M. Burt, "High speed differential protection for smart DC distribution system," *IEEE Trans. Smart Grid*, vol. 5, no. 5, pp. 2610–2617, 2014.

[26] Z. Xu, B. Zhang, S. Sirisukprasert, X. Zhou, and A. Q. Huang, "Circuit breaker technologies for advanced ship power systems," in *Power Engineering Society Winter Meeting, 2002. IEEE*, 2002, pp. 288–293.

[27] R. Schmerda, S.Krstic, E. Wellner, and A. Bendre, "IGCTs vs. IGBTs for circuit breakers in advanced ship electrical systems," in *Electric Ship Technologies Symposium, 2009. ESTS 2009. IEEE*, 2009, pp. 400–405.

[28] S. D. A. Fletcher *et al.*, "Optimizing the roles of unit and non-unit protection methods within DC microgrids," *IEEE Trans. Smart Grid*, vol. 3, no. 4, pp. 2079–2087, Dec 2012.