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A modified cascade transformer-based multilevel inverter and its efficient switching function

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ABSTRACT

A modified multilevel PWM inverter is proposed to increase the number of output voltage levels and to improve the system characteristic of a prior 11-level shaped PWM inverter scheme. In appearance, it consists of three full-bridge modules and a cascade transformer; therefore, the configuration of the proposed multilevel PWM inverter is equal to that of the prior one. Only the turn-ratio of one transformer and its corresponding switching function are different from each other. Based on the difference, the proposed multilevel PWM inverter has two promising advantages. First, output voltage levels increase almost two-fold. Consequently, it can generate more sinusoidal output voltage waves. Second, due to a suitable switching pattern, it lightens power imposed on the transformer, which is used for compensating output voltages with chopped pulses between step levels. Operational principle of the proposed 19-level shaped PWM inverter is analysed with comparisons of the prior 11-level shaped PWM inverter. The validity of the proposed inverter system is verified by computer-aided simulations and experimental results based on a 1 kW prototype.

1. Introduction

Recently, multilevel inverters have appeared as a new breed of power converters. The main advantages of multilevel inverters include the increase of power, the reduction of voltage stress on the power switching devices, and the generation of high quality output voltages [1–3,10,11].

In the viewpoint of generation of high quality output voltage wave, we can consider three presentable topologies, i.e., diode-clamped (neutral clamped) [6,13–16], flying capacitors [17–21], and cascaded H-bridge cells with separate DC sources [8,22–26]. Theoretically, they can synthesize an infinite output voltage level. By increasing the number of levels in the inverter, the output voltage has more steps generating a staircase waveform, which has a reduced harmonic distortion. However, to generate a large number of levels using the conventional multilevel schemes, they require a lot of switching devices, clamping diodes, flying capacitors, and other components. It, moreover, causes to the increase of control complexity. Therefore, these conventional multilevel inverters are not suitable for increasing the output voltage levels [4–8]. To alleviate the aforementioned problem, a 3^n-level shaped inverter was suggested in [4,5,12]. The basic principle of the 3^n-level shaped inverter is that the continuous output voltage levels can be synthesized by addition or subtraction of the instantaneous voltages generated from a cascade transformer. It generates a large number of output voltage levels with minimized number of switching devices. However, a cascade transformer operating on low switching frequency causes the size and volume of system to increase. A modified $(3^{n-1}+2)$ level shaped PWM inverter was proposed for the use of photovoltaic system [9]. This multilevel scheme was implemented on 11-level and 29-level outputs. The $(3^{n-1}+2)$ level shaped inverter is divided into two inverter modules according to their peculiar functions. One is a level inverter assembly synthesizing basic output levels, and another is a pulse width modulated inverter to compensate voltage waves between step levels. By this operational separation, this approach can reduce the size of transformers in the case of 11-level PWM inverter scheme. However, total harmonic distortion of the 11-level PWM output voltage is not good at no-load and light load conditions.

In this paper, a revised multilevel PWM inverter employing an efficient switching function is presented. It is useful to increase of the number of output voltage level ensuring high quality output voltages. Thanks to an effective switching pattern, it lightens power imposed on the transformer, which is used for compensating output voltages with chopped pulses operated on high switching frequency. We make an analysis of the proposed multilevel PWM inverter comparing with the prior $(3^{n-1}+2)$ level inverter. The performance of the proposed inverter system is verified by

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computer-aided simulations and experimental results based on a 1 kW prototype.

2. Comparison of proposed 19-level PWM inverters with prior 11-level PWM inverter

2.1. The difference in configuration

Fig. 1(a) shows the circuit configuration of the prior $(3^{n-1}+2)$ level shaped PWM inverter in case of $n=3$ and Fig. 1(b) shows the proposed multilevel PWM inverter. For the sake of convenience, Fig. 1(a) and (b) are entitled as an 11-level shaped PWM inverter and proposed 19-level shaped PWM inverter, respectively. Both inverters are same in their appearances. They are consisted of three full-bridge inverters and a cascade transformer. The differences between them are the turn-ratio of one transformer (Tr.1) and corresponding switching functions. Among full-bridge inverters, two-level inverters synthesize fundamental output voltage levels, and a PWM inverter generates chopped pulses to compensate output voltage wave between step levels. Owing to these differences, the proposed 19-level PWM inverter has two promising advantages. First, the number of output voltage levels increases almost two-fold; it guarantees more sinusoidal output voltage waveform. Second, due to a revised switching pattern, it lightens power imposed on the transformer, which is used for compensating output voltages with chopped pulses between steps. Because the PWM inverter linked with the transformer (Tr.1) is operated on high switching frequency for chopping operation. Note that the PWM inverter connected to Tr.1 focuses on an improvement of output voltage wave rather than power transfer.

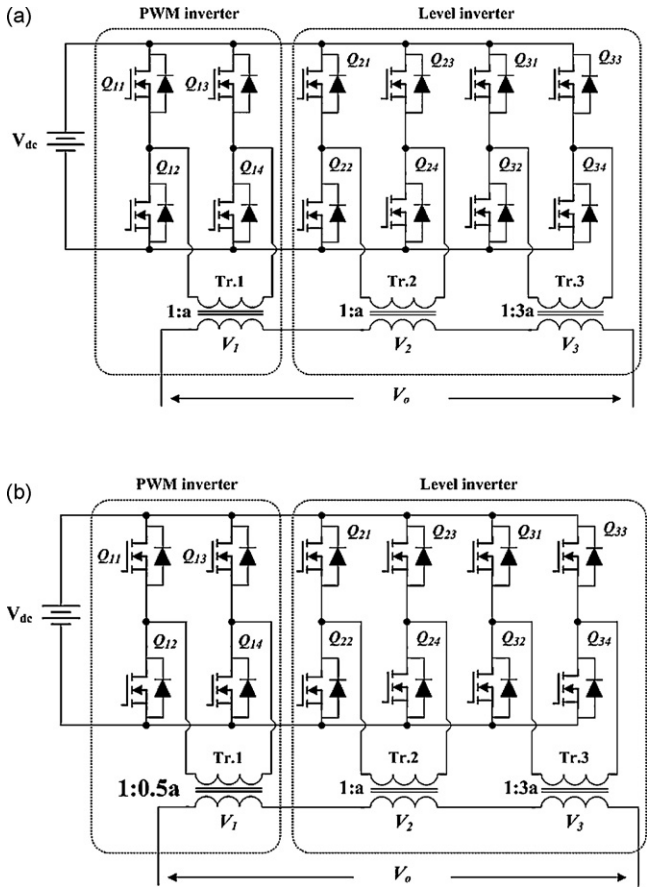

Fig. 1. Circuit configurations, (a) prior 11-level shaped PWM inverter, (b) proposed 19-level shaped PWM inverter.

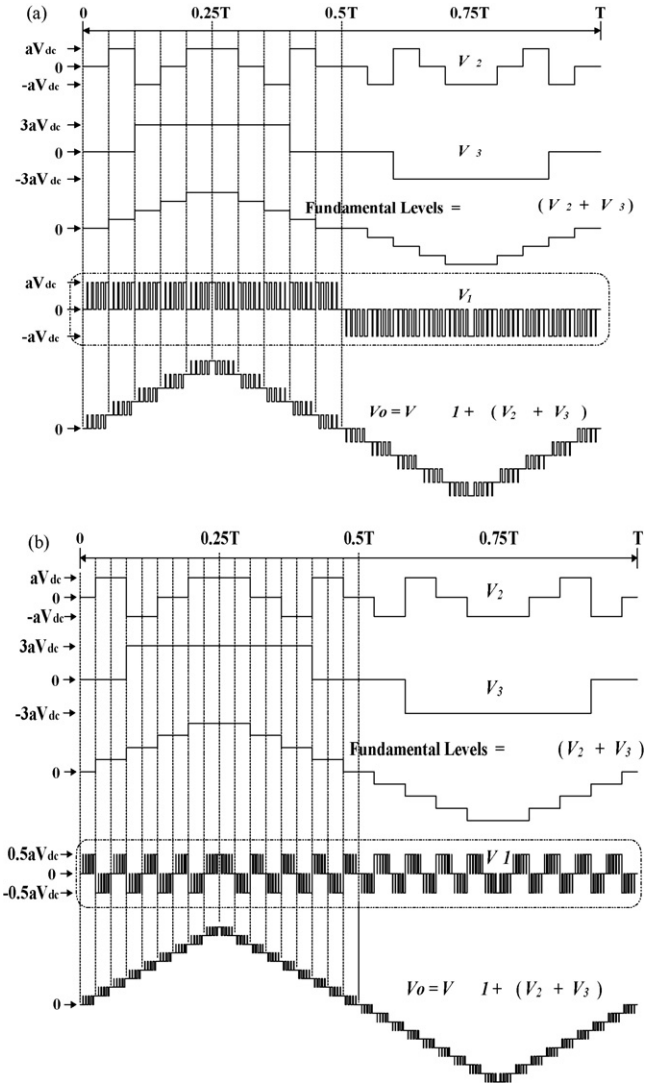

Fig. 2. Operational waveforms, (a) prior 11-level shaped PWM inverter, (b) proposed 19-level shaped PWM inverter.

2.2. The difference in operational principle

Fig. 2(a) and (b) show key waveforms of the prior 11-level shaped PWM inverter and the proposed 19-level shaped PWM inverter, respectively. Each of them shows terminal voltages of level inverters (V_2, V_3), a terminal voltage (V_1) of PWM inverter, and a final output voltage (V_o) in sequence. Both of the fundamental output

Table 1
Comparison of output level by combination of transformers.

Cascaded Transformers	Tr. 1	Tr. 2	Tr. 3	Tr. 4	··· Tr. *n*
Turns ratio	1:a / 1:0.5a	1:a	1:3a	1:9a	··· 3^{n-1}a 1
Output Levels	3-level	5-level	7-level	11-level	19-level
				19-level	29-level
				29-level	55-level
11-level shaped					(1)
19-level shaped					(2)

Table 2
Switching function of prior 11-level shaped PWM inverter.

Output level	Switching function			Terminal voltage			Output voltage
	SF_1	SF_2	SF_3	V_1	V_2	V_3	V_o
0	0	0	0	0	0	0	0
1	$0 \leftrightarrow 1$	0	0	$0 \leftrightarrow a\,V_{dc}$	0	0	$a\,V_{dc}$
2	$0 \leftrightarrow 1$	1	0	$0 \leftrightarrow a\,V_{dc}$	$a\,V_{dc}$	0	$2a\,V_{dc}$
3	$0 \leftrightarrow 1$	−1	1	$0 \leftrightarrow a\,V_{dc}$	$-a\,V_{dc}$	$3a\,V_{dc}$	$3a\,V_{dc}$
4	$0 \leftrightarrow 1$	0	1	$0 \leftrightarrow a\,V_{dc}$	0	$3a\,V_{dc}$	$4a\,V_{dc}$
5	$0 \leftrightarrow 1$	1	1	$0 \leftrightarrow a\,V_{dc}$	$a\,V_{dc}$	$3a\,V_{dc}$	$5a\,V_{dc}$

levels ($V_2 + V_3$) are same as a nine-level. The difference between 11-level shaped PWM inverter and 19-level shaped PWM inverter occurs in the waveform of V_1 as depicted in Fig. 2. In case of Fig. 2(a), the level inverters synthesize a fundamental nine-level including a zero-level while the PWM inverter adds chopped two-level pulses to the fundamental level. So the final output voltage becomes a pulse width modulated 11-level wave. The polarity of V_1 depends on that of final output voltage (V_o). Therefore, operating frequency of Tr.1 is nearly same with output frequency. So it requires a somewhat large transformer, which is operated on low switching frequency. In case of Fig. 2(b), the level inverters synthesize a fundamental nine-level including a zero-level without discrimination, and the PWM inverter adds chopped two-level pulses to the fundamental level. However, V_1 alternately changes its polarity at every step. As a result, output voltage levels increase about two-fold compared with the case of Fig. 2(a). Intuitively, we can find that a basic operating frequency of V_1 depicted in Fig. 2(b) is 17 times as high as that of Fig. 2(a). Therefore, the transformer (Tr.1) can be designed as a high frequency transformer with a reduced core size. Moreover, this switching scheme reduces the power distribution imposed on Tr.1. It is desirable that most power is transferred to load via the transformers (Tr.2 and Tr.3), which play a role to synthesize the fundamental output level. Note that the objective of the PWM inverter is to improve the output voltage rather than to transfer energy to loads.

Table 1 shows a comparison of output voltage level by combination of cascaded transformers. The number of output level for the prior 11-level shaped PWM inverter and the proposed one is normalized by (1) and (2), respectively. Here n means the number of selectable transformers in sequence.

$$N_{11} = 3^{n-1} + 2, \quad n = 1, 2, 3 \ldots \tag{1}$$

$$N_{19} = 2 \times 3^{n-1} + 1, \quad n = 1, 2, 3 \ldots \tag{2}$$

On the whole, the proposed 19-level shaped PWM inverter is more useful to synthesize output levels.

Table 3
Switching function of proposed 19-level shaped PWM inverter.

Output level	Switching function			Terminal voltage			Output voltage
	SF_1	SF_2	SF_3	V_1	V_2	V_3	V_o
0	0	0	0	0	0	0	0
1	$0 \leftrightarrow 1$	0	0	$0 \leftrightarrow 0.5a\,V_{dc}$	0	0	$0.5a\,V_{dc}$
2	$0 \leftrightarrow -1$	1	0	$0 \leftrightarrow -0.5a\,V_{dc}$	$a\,V_{dc}$	0	$LOa\,V_{dc}$
3	$0 \leftrightarrow 1$	1	0	$0 \leftrightarrow 0.5a\,V_{dc}$	$a\,V_{dc}$	0	$1.5a\,V_{dc}$
4	$0 \leftrightarrow -1$	−1	1	$0 \leftrightarrow -0.5a\,V_{dc}$	$-a\,V_{dc}$	$3a\,V_{dc}$	$2.0a\,V_{dc}$
5	$0 \leftrightarrow 1$	−1	1	$0 \leftrightarrow 0.5a\,V_{dc}$	$-a\,V_{dc}$	$3a\,V_{dc}$	$2.5a\,V_{dc}$
6	$0 \leftrightarrow -1$	0	1	$0 \leftrightarrow -0.5a\,V_{dc}$	0	$3a\,V_{dc}$	$3.0a\,V_{dc}$
7	$0 \leftrightarrow 1$	0	1	$0 \leftrightarrow 0.5a\,V_{dc}$	0	$3a\,V_{dc}$	$3.5a\,V_{dc}$
8	$0 \leftrightarrow -1$	1	1	$0 \leftrightarrow -0.5a\,V_{dc}$	$a\,V_{dc}$	$3a\,V_{dc}$	$4.0a\,V_{dc}$
9	$0 \leftrightarrow 1$	1	1	$0 \leftrightarrow 0.5a\,V_{dc}$	$a\,V_{dc}$	$3a\,V_{dc}$	$4.5a\,V_{dc}$

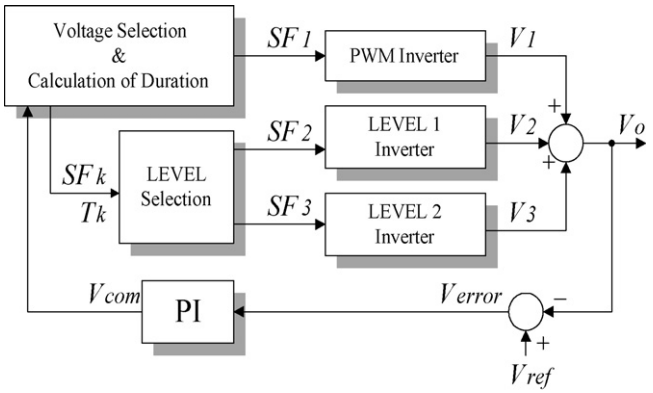

Fig. 3. Control block diagram of the proposed multilevel inverter.

2.3. The difference in switching function

Table 2 shows switching functions of the prior 11-level shaped PWM inverter for generating positive output voltages [9]. Table 3 shows switching functions for the proposed one. For a negative case, switching functions of each inverter is obtained by multiplying −1 to Table 2 and Table 3, respectively. Based on both tables, each switching function is given by using C-language expressions. Here all variable are assumed integers. % is the modulus operator, and || is the logical operator OR. In Table 2, switching function for the PWM inverter (SF_1) is given as

$$\text{if } (n > 0) \quad \text{then} \quad SF_1 = \langle 0 \leftrightarrow 1 \rangle \tag{3}$$

$$\text{if } (n = 0) \quad \text{then} \quad SF_1 = 0 \tag{4}$$

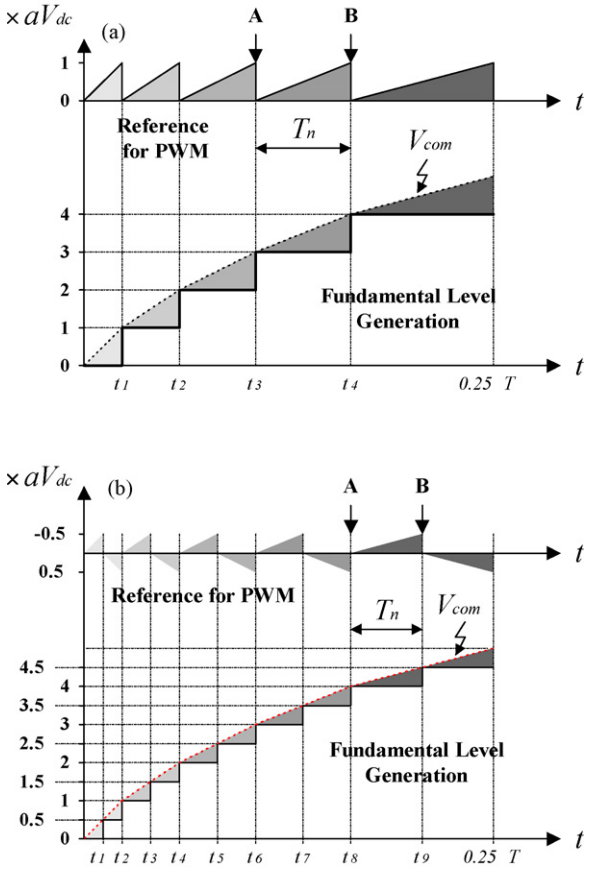

Fig. 4. Determination of output level and its duration, (a) prior 11-level shaped inverter, (b) proposed 19-level shaped inverter.

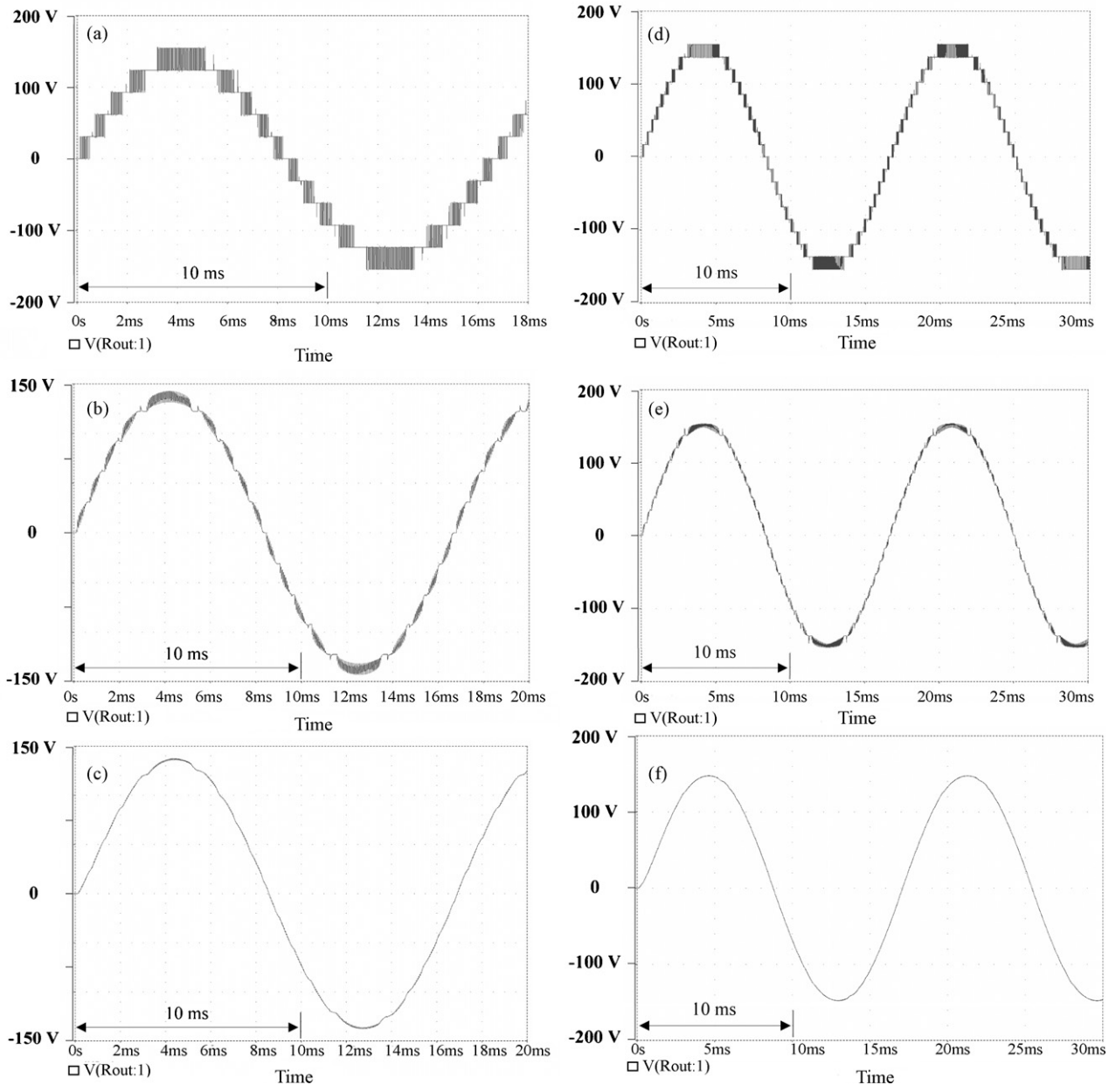

Fig. 5. Simulation results of output voltage according to the increase of load power, (a) 11-level shaped PWM inverter; no-load, (b) 11-level shaped PWM inverter; 500 W, (c) 11-level shaped PWM inverter; 1 kW, (d) proposed 19-level shaped PWM inverter; no-load, (e) proposed 19-level shaped PWM inverter; 500 W, (f) proposed 19-level shaped PWM inverter; 1 kW.

On the other hand, switching function for the PWM inverter (SF_1) of the proposed 19-level shaped PWM inverter is defined by

$$\text{if } (n\%2 = 1) \quad \text{then} \quad SF_1 = 1 \tag{5}$$

$$\text{if } (n\%2 = 0) \quad \text{then} \quad SF_1 = 1 \tag{6}$$

In case of the prior inverter, SF_1 plies between 0 and 1 whereas SF_1 of the proposed inverter iterates from 1 to −1. Because the result of the new switching function (SF_1) listed in Table 3, the proposed multilevel inverter sprits each step into two levels. So it can increase output levels twice compared with the prior multilevel inverter scheme. Switching function (SF_2) for the first level inverter of the prior scheme is given as

$$\text{if } (n\%3 = 0) \quad \text{then} \quad SF_2 = 1 \tag{7}$$

$$\text{if } [(n\%3 = 1)||(n = 0)] \quad \text{then} \quad SF_2 = 0 \tag{8}$$

$$\text{if } (n\%3 = 2) \quad \text{then} \quad SF_2 = 1 \tag{9}$$

The switching function (SF_3) of the prior approach takes a naught when an output level is lower than the third level. In contrast, it takes a unity when a required level is equal or higher than the third level. Therefore, SF_3 is written as

$$\text{if } (n < 3) \quad \text{then} \quad SF_3 = 0 \tag{10}$$

$$\text{if } (n \geq 3) \quad \text{then} \quad SF_3 = 1 \tag{11}$$

In case of the proposed scheme, switching function (SF_2) of the first level inverter is expressed as

$$\text{if } [((n+2)/2)\%3 = 0] \quad \text{then} \quad SF_2 = -1 \tag{12}$$

$$\text{if } [((n+2)/2)\%3 = 1] \quad \text{then} \quad SF_2 = 0 \tag{13}$$

$$\text{if } [((n+2)/2)\%3 = 2] \quad \text{then} \quad SF_2 = 1 \tag{14}$$

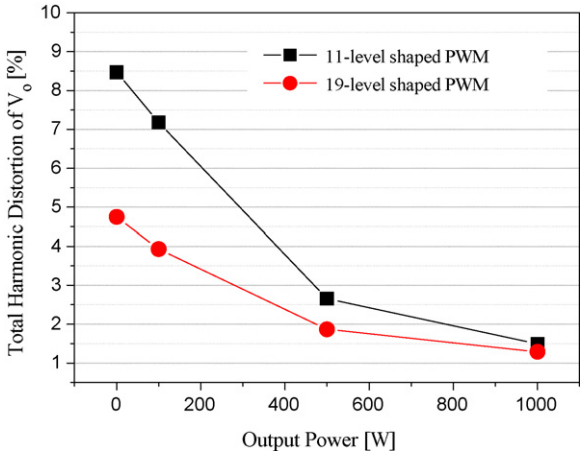

Fig. 6. Comparison of total harmonic distortion.

From Table 3, SF_3 is given as

$$\text{if } (n < 4) \quad \text{then} \quad SF_3 = 0 \tag{15}$$

$$\text{if } (n \geq 4) \quad \text{then} \quad SF_3 = 1 \tag{16}$$

The switching function (SF_3) of the proposed method takes a naught when an output level is lower than the fourth level. And it takes a unity when a command level is equal or higher than the forth level.

SF_n is the switching function of the full-bridge inverter, so it has three different states, i.e., 1, 0, and −1, respectively. Then, the output voltage of the prior 11-level shaped PWM inverter is defined by

$$V_{o\_11} = a[SF_1 + SF_2 + 3SF_3]V_{dc} \tag{17}$$

The output voltage of the proposed 19-level shaped PWM inverter yields

$$V_{o\_19} = 0.5a\,[SF_1 + 2SF_2 + 6SF_3]\,V_{dc} \tag{18}$$

2.4. Determination of output level and duration

Fig. 3 shows a simplified control block diagram for the proposed 19-level shaped PWM inverter. Based on a feedback signal of an output voltage (V_o) and a reference signal (V_{ref}), command voltage (V_{com}) is obtained using a general PI control. V_{com} determines a proper voltage level and its duration.

Fig. 4 shows the idea to determine output voltage level and corresponding duration. Basically, both methods are same except the number of split level. In case of 11-level outputs, a quarter of a cycle is divided into four levels with the same height whereas the proposed scheme separates that same period into nine levels. By comparing the nine levels with V_{com}, the beginning and ending point is set to determine duration of each level. For example, in Fig. 4(b) the crossing point (A) between V_{com} and the eighth level becomes the starting point of duration (t_9–t_8), and the next crossing point (B) between V_{com} and one-level increased ninth level finishes the duration. During the same duration, PWM pulses (plying between 0 and 0.5, alternately) are proportionally increased their width to make output voltage more sinusoidal. A case where it goes the next level, PWM pulses are iterated from 0 to −0.5 as depicted in Fig. 4(b).

Table 4
Specification of the prototype.

Items	Specifications and features
Switches	Power MOFET (FS100UMJ03) 30 V/100a
Cascade transformer	EI lamination; here, $\alpha = 2\sqrt{2}$ Tr.1 (1:0.5a), Tr.2 (I:a), Tr.3 (1:3a)
Battery (V_{dc})	PTI00BR 12 V/100 A
Output (V_o)	100 V_{ac}/60 Hz/1000 W

2.5. Comparison of power distribution per transformer

In the viewpoint of that the objective of the PWM inverter is to improve the output voltage rather than to transfer energy to load. The lighter power allotment on Tr.1 is more desirable. All circuit components including transformers are ideal so (19) did not consider on the power losses which are expected by switching losses, conduction losses, and other power losses. Then power allotted to each transformer is determined by the secondary turn-ratio of the transformer. It is normalized by

$$P_{Tr\_k} = \frac{T_{Sec\_k}}{\sum_{n=1}^{k} T_{Sec\_n}} \times 100 \quad (\%) \tag{19}$$

where T_{Sec_n} is the secondary turn-ratio of each transformer. Using (19), the rate of power distribution per transformer in the prior

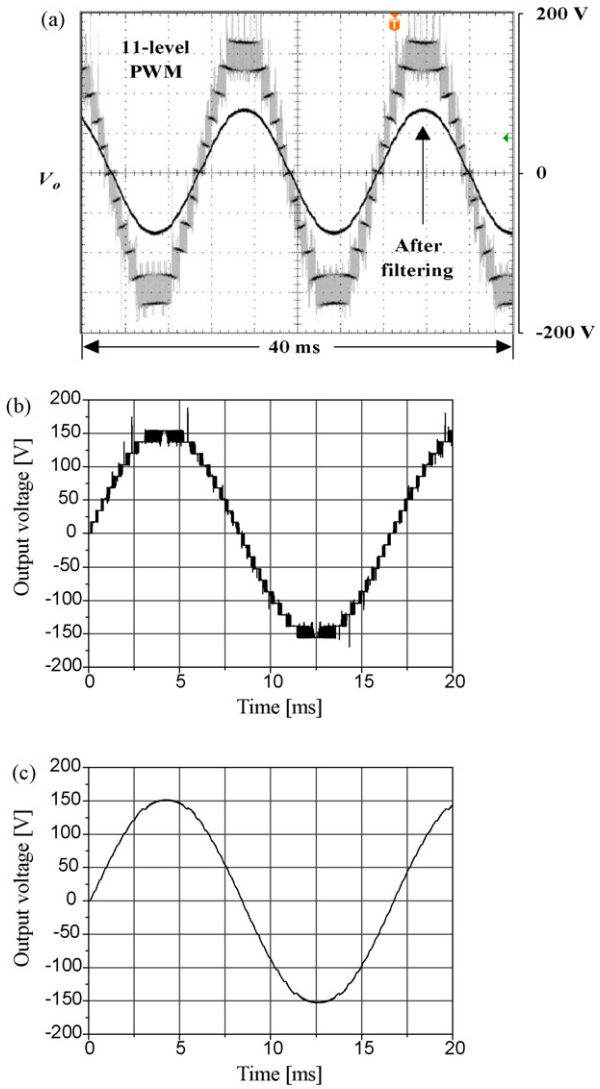

Fig. 7. Experimental results, (a) output voltage of the prior 11-level PWM inverter at no-load with superimposed filtered output voltage waveform, (b) output voltage of the proposed 19-level PWM inverter at no-load, (c) output voltage of the proposed 19-level PWM inverter at 1 kW load.

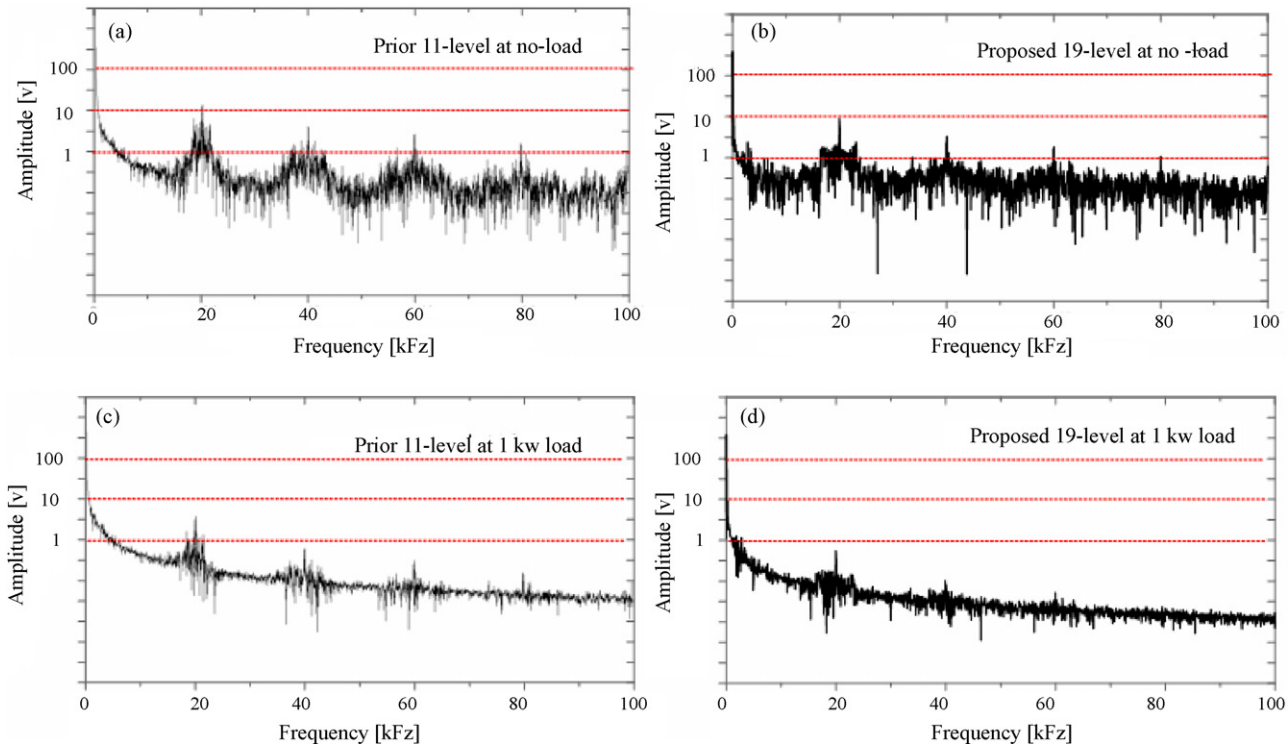

Fig. 8. Comparison of power spectrum to output voltage, (a) prior 11-level approach at no-load, (b) proposed 19-level approach at no-load, (c) prior 11-level approach at 1 kW load, (d) proposed 19-level approach at 1 kW load.

11-level shaped PWM inverter is calculated as

$$P_{TR\_1} = \frac{a}{(1+1+3)a} \times 100 = 20 \quad (\%) \tag{20}$$

$$P_{TR\_2} = \frac{a}{(1+1+3)a} \times 100 = 20 \quad (\%) \tag{21}$$

$$P_{TR\_3} = \frac{3a}{(1+1+3)a} \times 100 = 60 \quad (\%) \tag{22}$$

In case of the proposed one, the rate of power imposed on each transformer is determined by

$$P_{TR\_1} = \frac{0.5a}{(0.5+1+3)a} \times 100 = 11.11 \quad (\%) \tag{23}$$

$$P_{TR\_2} = \frac{a}{(0.5+1+3)a} \times 100 = 22.22 \quad (\%) \tag{24}$$

$$P_{TR\_3} = \frac{3a}{(0.5+1+3)a} \times 100 = 66.67 \quad (\%) \tag{25}$$

By comparison of (20) with (23), we can notice that the rate of power distribution of Tr.1 is decreased about 10%. This is promising result because the transformer (Tr.1) focuses on the improvement of output voltage wave rather than power transferring. Note that the inverter connected to Tr.1 has high switching frequency for chopping operation.

3. Simulation and experiment results

To assess the performance of the proposed 19-level shaped PWM inverter scheme, we first implemented a computer-aided simulation using PSpice. The simulation results are compared with that of the prior 11-level shaped PWM inverter. In the simulation, the switching frequency of the PWM inverter is set to 20 kHz. Coupling coefficient of each transformer is set to 0.99 while other nonlinear stray components are ignored. A resistive load is applied for the simulation. Fig. 5 shows simulation results of output voltage. Critical levels appearing PWM wave are shown in both cases (Fig. 5(a) and (d)) at a no-load condition. However, it is changed into sinusoidal wave with the increase of load power. The leakage inductance of the cascade transformer plays a role to filter off high-order harmonic components.

Fig. 6 shows the rate of THD (total harmonic distortion). It is a simulation result considered on 100th order harmonic components. In case of the proposed 19-level shaped PWM inverter, it meets the general THD requirement of 5% below in all ranges of the power rating. However, the prior 11-level shaped PWM inverter does not satisfy that regulation at no-load and light load conditions. Therefore, it requires an output filter to improve THD of the output voltage at no-load and light load conditions.

In experiment, a 12 V battery is used as an input voltage source, and the output voltage is 100 V. The output frequency is 60 Hz. The controller is DSP (TMS320F241). Table 4 shows the specification of the prototype. Fig. 7(a) shows experimental results of the prior 11-level PWM inverter at no-load. It also shows filtered output voltage. Fig. 7(b) and (c) show output voltage waveforms of the proposed 19-level shaped PWM inverter. They were measured at no-load and 1 kW resistive load conditions, respectively. From the voltage waveform shown in Fig. 7(b), an accurate 19-level is appeared in the output voltage wave. In case of a no-load condition, output voltage of the proposed inverter is more close to sinusoidal wave compared with that of the prior 11-level shaped PWM inverter scheme given in Fig. 7(a). It is a matter of cause because the output level of the proposed inverter is almost twice as much as the prior one. Fig. 7(c) shows the output voltage of the proposed 19-level shaped PWM inverter at 1 kW load. In this figure, it is difficult to find a step variation of each level because output voltage levels are collapsed by the effect of filtering of the cascade transformer. From these results, we can know that the proposed multilevel PWM inverter scheme largely depends on the load power condition. Fig. 8 shows power spectrum results of the output voltage. Fig. 8(a) is the power spectrum of the output voltage of the prior 11-level PWM inverter at

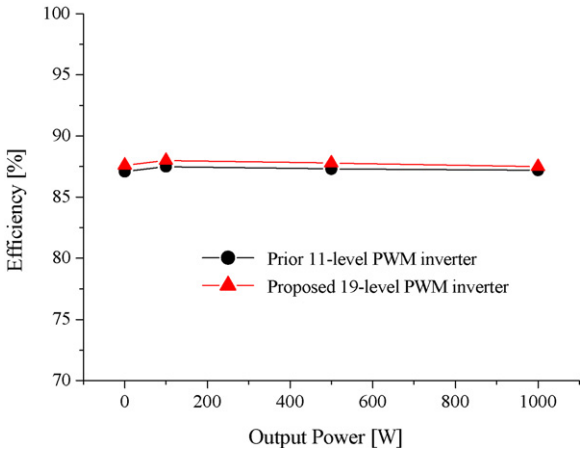

Fig. 9. Efficiency comparison.

no-load. Fig. 8(c) is the spectrum result of the prior 11-level PWM inverter at a rated load. Fig. 8(b) and (d) are power spectrum results of Fig. 7(b) and (c), respectively. From Fig. 8(d), it is more clearly proved that the effect of filtering by means of the cascade transformer. From Fig. 8, we can notice that the proposed 19-level shaped PWM inverter scheme shows better characteristics in the reduction of dv/dt stresses.

Fig. 9 shows the efficiency comparison graph. In this figure, the average efficiency of the prior 11-level inverter is measured 87.275% and the proposed 19-level inverter shows 87.725%. The proposed inverter shows about 0.513% improvements in system efficiency. Actually, both inverters show almost the same efficiency. We can notice that the proposed 19-level PWM inverter is suitable for improving THD of the output voltage, but efficiency does not improved significantly.

4. Conclusion

A modified multilevel PWM inverter entitled as 19-level shaped PWM inverter was presented. The circuit configuration of the proposed multilevel inverter is equal to that of the prior 11-level shaped PWM inverter. Only the turn-ratio of a transformer and its corresponding switching function are different from each other. Owing to the modification, the number of output voltage levels of the proposed multilevel inverter becomes almost twice as much as that of the prior 11-level shaped PWM approach. As a result, it can meet a general output voltage THD requirement 5% below at no-load and light load conditions without an additional filter. To verify the validity of the proposed multilevel scheme, we implemented computer-aided simulations and experiments using a prototype.

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