# Fault Protection Scheme for DC Nanogrids Based on the Coordination of Fault-Insensitive Power Electronic Interfaces and Contactors

Saroosh Saeed and Luiz A.C. Lopes
Department of Electrical and Computer Engineering
Concordia University, Montreal, QC, Canada.
saroashsaeed78@hotmail.com, lalopes@encs.concordia.ca

***Abstract*— DC microgrids can lead to a better integration of Distributed Energy Resources (DERs) than AC microgrids. DC nanogrids typically include a number of DERs in close proximity. Various power balance and energy management schemes have been developed, but fault protection still remains an issue for DC nanogrids. This paper discusses the realization of a fault detection and isolation scheme based on the coordination of fault-insensitive power electronic interfaces and low-cost contactors. It is based on "local branch current sensing" and peer-to-peer communication to identify which segment of the DC nanogrid is faulted and which contactor should open. In order to employ low cost/current contactors, following the detection of a fault, the DERs should decrease the injected current to a value low enough for safe action of the contactors. For that, a fault-insensitive current controller power electronics interface as discussed in this paper is needed. Experimental results with power electronics interfaces operating with DC Bus Signaling (DBS) and a CAN communication scheme are presented.**

**Keywords—DC-nanogrid, distributed energy resources, fault-insensitive converter, protection scheme, CAN communication**

## I. INTRODUCTION

The bidirectional class C DC-DC converter shown in Fig. 1 is frequently employed as the interface of Energy Storage Systems (ESSs) in DC nano and microgrids [1]. It is a simple and effective topology, but it is expected to operate with an input (storage medium) voltage lower than the output (DC bus) voltage, what is fine for normal operating conditions. However, it is a fault-sensitive converter, meaning that in case of a fault in the DC bus, with an output voltage lower than the input voltage, the upper anti-parallel diode conducts. Thus, one loses control of the current injected into the DC grid, which tends to increase significantly. This is not an issue in conventional DC microgrids that employ expensive high current DC Circuit Breakers (CBs). Protection coordination is relatively simple due to the non-negligible feeder impedance between DERs.

The challenge in DC nanogrids with multiple Distributed Energy Resources (DERs) is the difficulty in making only the DC CBs close to the fault to open [2], [3]. Available fault protection techniques, include rate of current rise (ROCR) protection [4], distance protection [5] and signal processing based protection [6]. These are fine for large systems, but the low impedances between nodes in DC nanogrids make it difficult to achieve high levels of discrimination.

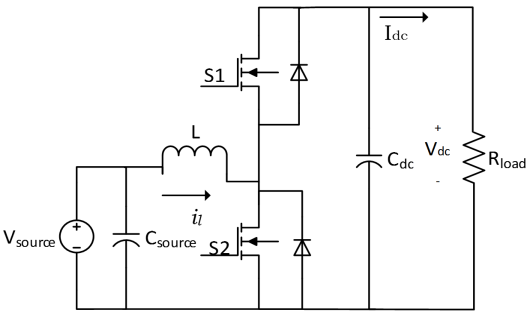


Fig. 1. (DC bus) fault-sensitive bi-directional class C DC-DC converter.

An interesting concept proposed in [7] for DC ring-bus microgrids, is to replace the DC CBs with lower cost, but lower current, contactors and employ a logic to determine which contactors should be opened, to clear the faulted DC nanogrid segment. This can be determined based on the direction of the currents in the left and right branches at the point of connection of a DER. In order for the contactors to open with a low current, the power electronics interfaces of all DERs should be fault-insensitive. That is, capable of controlling the current injected into the DC nanogrid with an output (faulted DC bus) voltage lower than the input (storage medium) voltage. This can be done with a 4-switch converter [8], but the current control scheme was not detailed in there.

As discussed in [7], the DERs cannot be connected directly to the DC distribution system when such a protection scheme is used. It requires a *DER interface node*, shown in Fig. 2, which consists of two sets of a current sensor in series with a contactor. The current sensors provide the information regarding magnitude and direction of the current in their branches to a digital controller which can be the same as that of the power electronics interface. The digital controllers of neighboring DERs communicate with each other on a peer-to-pear fashion the information regarding the currents in the common branch. In case of a fault, the digital controllers of the power electronics interface and *DER interface nodes*, should reduce the injected

978-1-7281-4878-6/19/$31.00 ©2019 IEEE

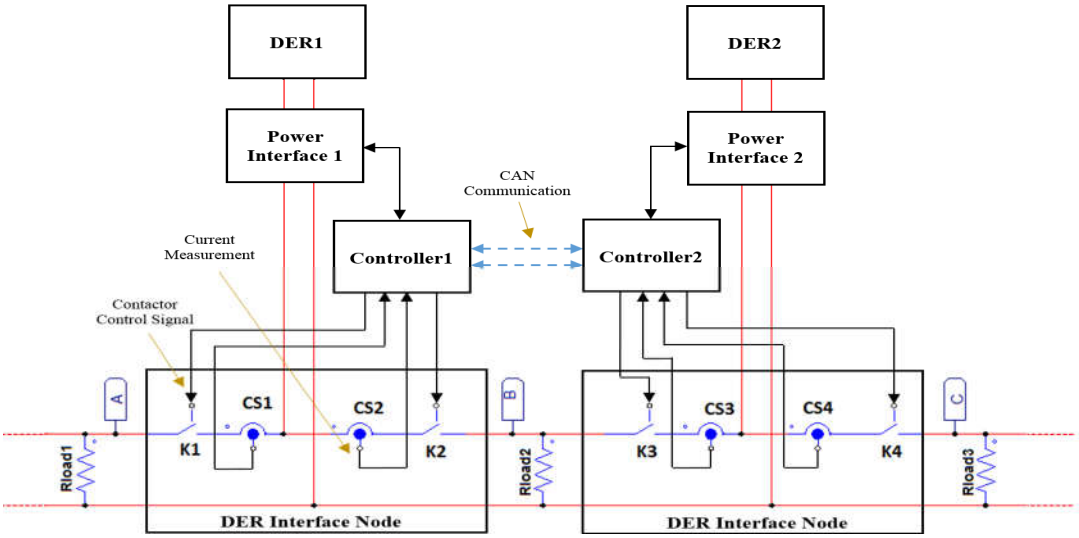



Fig. 2. Generic DC nanogrid segment with power electronic interfaces, *DER interface nodes* and load groups.

current and based on a suitable logic decide to open one or none of their contactors.

This paper presents a current control scheme for a fault-insensitive 4-switch converter that operates as a class C converter under normal conditions and in the Buck mode under faulted conditions. This is added to the conventional DC Bus Signaling (DBS) control scheme of DERs typically used in DC nano and microgrids [9]. Besides, the overall fault protection logic is realized in an experimental DC nanogrid with two DERs and three load nodes. This includes the DER interface nodes, peer-to-peer communication scheme, a complete storage unit and 4-switch power electronics interface as well as an "emulated DER with droop control and current limiting," realized with a DC power supply and series (droop) resistor. A number of experimental tests are presented to verify the performance of the actual and the emulated DER. First individually, then in the DC nanogrid with the two DERs, communication scheme and *DER interface nodes*, subject to all individual node faults.

## II. The Fault-Insensitive Power Electronics Converter And The Current Control Loop

The (DC bus) fault-insensitive power electronics converter used in this work is based on the 4-switch bidirectional DC-DC converter shown in Fig. 3.a) connected to a DBS-controlled nanogrid [10]. S2 operates complementarily to S1 and S4 to S3. Under "normal conditions," it operates in the class C mode, with S1 ON while S4 is switched with Pulse-Width Modulation (PWM) to regulate the inductor current ($I_L$). Under "faulted conditions," it operates in the Buck mode, with S3 ON while S1 is switched with PWM to regulate $I_L$. The reference value for $I_L$, is obtained from the reference value of the injected/output current ($I_{out}$). Neglecting the converter losses, the reference value of $I_L$ (= $I_{in}$) is obtained using the power conservation principle ($P_{in} = P_{out}$) from the reference value of $I_{out}$.

It is assumed that the DERs operate with DBS. In such a case, $I_{out}$ is based on the local/terminal DC bus voltage ($V_{dc}$) and a VI curve. The one shown in Fig. 3.b) and used in this work presents a droop segment, for $V_{dc} > V_{fl}$, the full-load DC bus voltage, and a current limiting segment. For $V_{dc} < V_{fl}$, the injected current is limited to a maximum nominal value ($I_{dc\_max}$). In case $V_{dc} < 0.5V_{fl}$ with $I_{out} = I_{dc\_max}$, this configures a "fault", what requires the 4-switch converter to operate in the Buck mode. This occurs after a small delay time to prevent false "fault-detection." Then, the reference value for $I_{out}$ decreases to a *low value* ($I_{dc\_lcl}$), so that the contactors can be opened with a safe current.

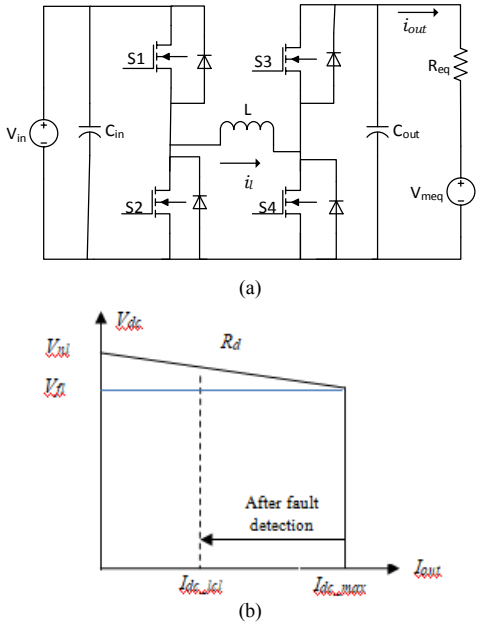



Fig. 3. Power electronics interface. (a) 4-Switch converter and equivalent model of a DC bus with a load and DERs operating with DC Bus Signaling (DBS). (b) VI curve of the DBS scheme for this interface.

The schematic diagram depicted in Fig. 4 shows how to generate the gating signals of the 4-switch converter, so as to track the reference inductor current under normal and faulted conditions. $V_{mode}$ is "0" for operation in the normal modes as a class C converter. In such a case, S1 remains ON all the time while S4 operates with PWM according to the modulating signal produced by the current PI controller. $V_{mode}$ is "1" for operation in the faulted condition in the Buck mode. This leads S3 to remain ON all the time, while S1 operates with PWM. The $V_{mode}$ (fault) signal is determined as described in the previous paragraph. Further details, including the transfer function of the "plant" for both modes of operation and the design of a single PI type controller, are presented in [11].

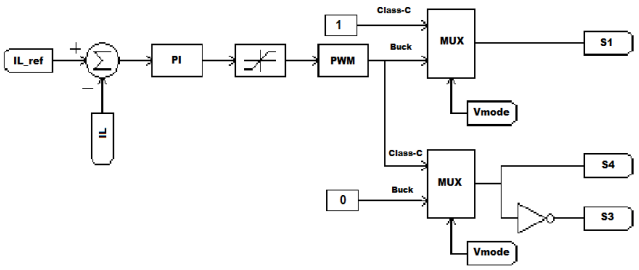



Fig. 4. Schematic diagram of the fault-insensitive current controlled 4-switch converter for operation under normal (class C) and faulted (Buck) conditions.

## III. THE *DER INTERFACE NODE* AND LOGIC FOR DETERMINING THE CONTACTORS TO OPEN

As mentioned before, the *DER interface nodes* sense the magnitude and direction of the currents in their branches to the right and to the left and send this information to the digital controller of the DER. By definition, as shown in Fig. 2, the sensor and contactor to the left branch have an odd number and those to the right branch have an even number. By peer-to-peer communication, a DER, say DER2, sends to its neighbor to the left, (DER1) a fault signal ($V_{mode2}$) and the direction of the current in its left branch, sensed by CS3. $B_{CS3} = 1$ if the current flows from left to right and $B_{CS3} = 0$ if the current flows from right to left. From the neighbor to the left (DER1), DER2 also receives the information regarding the neighbor's fault signal ($V_{mode1}$) and current in his right side branch. That is, of current sensor 2 (CS2). If there is a fault in the branch between these two DERs, $V_{mode1} = V_{mode2} = 1$, $B_{CS2} = 1$ and $B_{CS3} = 0$, what should lead to the opening of contactors K2 and K3. If the data communicated between the two DERs are identical, say $B_{CS2} = B_{CS3} = 1$ what should occur for currents flowing from left to right, then the fault is not in their common branch and those contactors should remain on. The fault might be in the immediate branch to the right side of DER2, what should be detectable by comparing the status of "his" $B_{CS4}$ to the right-side neighbor's $B_{CS5}$, not shown in Fig. 2. If they are identical, there are no faults in any branches connected to DER2.

If there is no DER to the left (right) of a given unit, the logic for opening an odd (even) contactor is to assume that $V_{mode\_N-1}$ ($V_{mode\_N+1}$) = 1 and the signal from the current sensor of its neighbor DER is 0 (1). This logic is also useful in case of failure in the peer-to-peer communication.

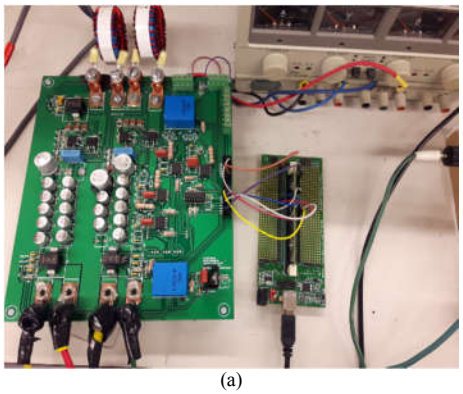
## IV. EXPERIMENTAL SET-UP

A 48 V DC nanogrid was implemented in the laboratory with two DERs and three load groups (A, B and C) of 60Ω as shown in Fig. 2. Table 1 presents the parameters concerning DBS and the current limits for normal/faulted conditions. A 48 V - 165 F supercapacitor from Maxwell was used as the storage unit.

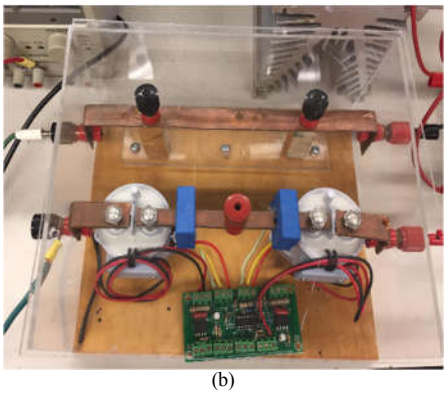
TABLE I. BASIC DATA OF THE DERS IN THE EXPERIMENTAL DC NANOGRID

| | |
|---|---|
| Source Voltage ($V_{DER}$) | 36 V |
| No-load voltage ($V_{nl}$) | 48 V |
| Droop Resistance ($R_d$) | 0.5 Ω |
| Full-load voltage ($V_{fl}$) | 45.5 V |
| Maximum current limit ($I_{dc\_max}$) | 5 A |
| Lower current limit at fault condition ($I_{dc\_lcl}$) | 2 A |
| Equivalent load resistance ($R_{load}$) | 20 Ω |

A 4-switch current-controlled converter capable of switching automatically from the class C mode (normal operation) to the Buck mode (faulted system) was implemented with MOSFETs and is controlled via a TMS320F28335. The code for the MCUs was generated with Code Composer Studio using PSIM. For peer-to-peer CAN communication, a transceiver SN65HVD230 was used. LA 55-P (LEM) Hall-effect current sensors and EV200 (TE Connectivity) contactors were used for implementing the *DER interface nodes*. Pictures of the 4-switch power converter and of the *DER interface nodes* are shown in Fig. 5.



(a)



(b)

Fig. 5. Power interface for the DC nanogrid. (a) 4-Switch converter and digital controller. (b) *DER interface node*.

## V. EXPERIMENTAL RESULTS

A number of experimental tests were conducted with the set-up. A single unit of the current-controlled 4-switch DC-DC converter was built. The other DER is emulated by means of a laboratory DC power supply with a current limit set at $I_{dc\_max}$. Operation of the emulated DER in the droop control mode is achieved with a series resistance equal to the droop slope ($R_d$). The voltage setting of the DC power supply corresponds to the no-load voltage ($V_{nl}$) of the DER. In the following sub-sections, first, the performance of the DERs (converter and power supply) is tested individually without *DER interface nodes* and communication. The objective is to observe their performance following a low impedance (fault) condition. Then, the complete system is implemented as shown in Fig. 2, with both DERs, *DER interface nodes* and peer-to-peer communication. This will allow the verification of the effectiveness of the fault location method, i.e., identify and open only the faulted segment. This is done by connecting a fault resistance ($R_{fault}$) of 1.1Ω at nodes A, B or C shown in Fig. 2.

### *A. Results with a single DER without DER interface nodes*

*4-switch converter following a low load impedance transition*

The transition of the 4-switch converter from the class C (normal) to the Buck (fault) mode of operation, following a load variation that makes $V_{dc} < 0.5V_{fl}$, is shown in Fig. 6. This test is conducted with a single DER, power electronic interface and load. In the beginning, the system is operating under droop control (load is 20Ω) in class C mode, as per the VI curve of the DC bus signaling, with S1 ON (dark blue curve) while S3 (light blue curve) regulates $I_L$, and consequently $I_{out}$, (green curve) with PWM. Following the connection of a low/fault impedance (2Ω) at the load bus, the current injected by the converter (green curve) increases very fast exceeding for a short time the maximum current ($I_{dc\_max}$). Recall that although the 4-switch converter can accurately control $I_L$, even with the DC bus voltage lower than the storage medium voltage, its output capacitor will provide an "unexpected" short peak current to the *fault impedance*, while it discharges.

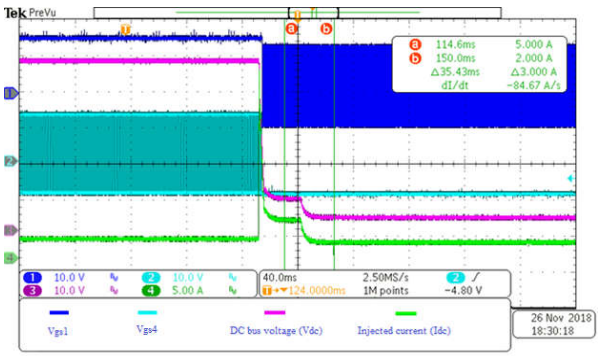



Fig. 6. Transition of 4-switch converter from class C to Buck. *Ch*1 (dark blue): $V_{gs1}$; *Ch*2 (light blue): $V_{gs4}$; *Ch*3 (pink): *DC bus voltage* ($V_{dc}$); *Ch*4 (green): *injected current* ($I_{dc}$ or $I_{out}$).

The DC bus voltage (pink curve) decreases to $V_{dc} < 0.5V_{fl}$ and the 4-switch converter changes from the class C to the Buck mode of operation. Thus, S1 starts to operate with PWM (dark blue curve) to regulate $I_L$ (green curve) while S3 is kept ON (light blue curve). After a user-settable time delay (30 ms in this test) with high output current ($I_{dc\_max}$) and low DC bus voltage, "fault" is detected and the converter starts to operate in the Buck mode at the lower current limit ($I_{dc\_lcl}$). This leads to a further decrease of the DC bus voltage (pink curve). The results show that the 4-switch converter is fault-insensitive with the proposed scheme for transitioning from "class C" to "Buck mode", being capable of controlling the injected current under normal as well as faulted DC grid conditions.

*Power supply following a low load impedance transition*

An "emulated DER-interface with droop control and current limiting" was built with a lab power supply and series droop resistor. Its response following a low load impedance transition is shown in Fig. 7. In the beginning, with low load current (load is 20Ω), the system operates under droop control as per the VI curve of the DCS. Following the connection of a low/fault impedance (2Ω), the DC bus voltage (pink curve) decreases. The current injected by the power supply (green curve) increases, exceeding for a short time the maximum current ($I_{dc\_max}$). A peak current, which lasts about 20 ms, is observed. It is due to the control scheme of this particular power supply under transient conditions. However, the "steady state current" is 5A, as set in the current limit. This is a key aspect in the later assessment of the fault protection scheme for DC nanogrids operating with multiple droop controlled DERs.

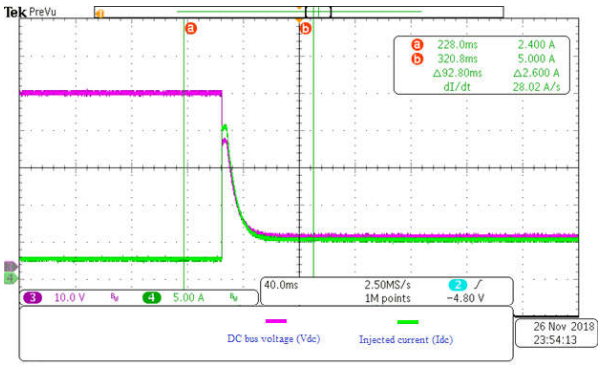



Fig. 7. Transient response of the power supply to a low load impedance transition. *Ch*3 (pink): *DC bus voltage* ($V_{dc}$); *Ch*4 (green): *injected current* ($I_{dc}$).

### *B. Results with the complete system*

In this sub-section, the results are shown for the complete system (DERs, *DER interface nodes* and communication) implemented as shown in Fig. 8, to verify the proposed fault protection scheme. There are three load nodes, all with 60Ω resistive loads and two DERs. DER2, at the right side, is the supercapacitor and the power interface 2 is the 4-switch converter. Conversely, DER1, at the left side, is the emulated DER consisting of a current limited DC power supply and series (droop) resistor. Since the DC power supply does not have an

accessible digital controller, its *DER interface node* is equipped with one so that it can communicate with the one from DER2.

As previously mentioned, the transient response of the DC power supply to a low load transition is about 20 ms. Therefore, for testing the fault detection and location scheme experimentally, this transient should be disregarded. Thus, once the fault occurs, an additional 50ms delay is introduced before starting the fault detection logic in the digital controllers. This is based on the magnitude and direction of the currents in the branches of the *DER interface nodes*. As the time for fault detection is 30ms, due to this delay, the total time will be 80 ms, the sum of 50ms (transient delay) and 30ms (settable delay time). Thus, the control signal for the contactors to open should be about 80 ms following the introduction of the fault impedance. With two actual DERs and 4-switch interfaces, the detection and contactor opening time could be limited to 30ms or less.

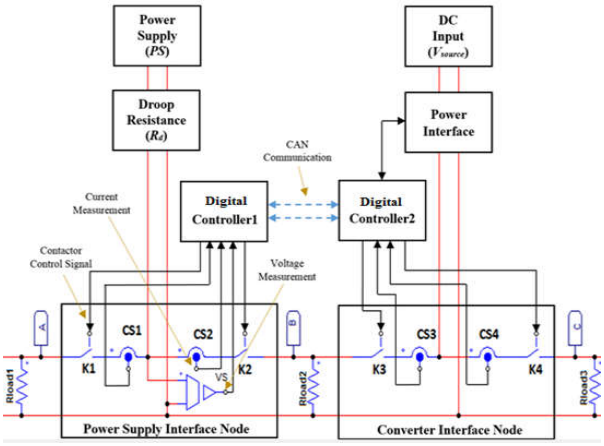



Fig. 8. Experimental system layout with emulated and actual DERs.

## *When a fault occurs at node 'A'*

The key waveforms of the system when a fault occurs at node 'A' are shown in Fig. 9. Initially, the system operate in normal load conditions with droop control. The DC bus voltage $V_{dc}$ (light blue curve), is 47.4V. Since the load resistances are identical (60Ω), they draw the same currents. One can say that $R_{load1}$ is fed by the power supply, $R_{load3}$ by the 4-switch converter and $R_{load2}$ by both. Hence, the currents that flow in CS2 and CS3 should be half of those in CS1 and CS4. As shown in Fig. 9, current $I_{cs1}$ (pink curve), is 800mA and $I_{cs2}$ (green curve) is 400mA. At $t$ = 80ms, a 1.1 Ω fault impedance is connected to node 'A'. Following a short transient, at $t$ = 120ms, the DC bus voltage decreases to 10.6V, both DERs start operating at maximum current limit (5A), $I_{cs1}$ and $I_{cs2}$ become -9.6A and -4.6A, respectively. The negative sign is due to the direction of the current flow, from right to left. Those values are not -10 A and -5 A, because there is also some current flowing to $R_{load2}$ and $R_{load3}$. At $t$ = 160ms, the fault condition is detected, as indicated by a fault flag (F) = 1, dark blue curve. The 4-switch converter starts operating at lower current limit ($I_{dc\_lcl}$ = 2A), what further decreases $V_{dc}$ (light blue curve). This lasts for 20 ms, until contactor K1 opens and isolates the faulted segment. After fault isolation, fault flag (F) = 0, the system returns to normal operation (droop control), $V_{dc}$ increases to 47.6V, higher than the pre-fault condition since only the loads at nodes B and C are fed by the DER. With K1 open, $I_{cs1} = 0A$ and $I_{cs2}$ = 800mA, positive sign since it flows from left to right, with the share of DER1 to supply identical loads $R_{load2}$ and $R_{load3}$, as shown in Fig. 9.

## *When a fault occurs at node 'B'*

The main waveforms of the system when a fault occurs at node 'B' are shown in Fig. 10. Again, in the beginning, the system is operating with droop control. The DC bus voltage $V_{dc}$, (light blue curve) is 47.4V, current $I_{cs2}$ (pink curve) is 409mA and $I_{cs3}$ (green curve) is –400mA. These are essentially the contributions of DER1 and DER2 to feed $R_{load2}$. At $t$ = 80ms, a 1.1 Ω fault impedance is connected to node 'B'. Following a short transient, $V_{dc}$ decreases to 10.5V, with both DERs operating at maximum current limit (5A). $I_{cs2}$ rises to 4.8A and $I_{cs3}$ falls to -4.8A. The remainder of the 5A current supplied by DER1 and DER2 go to $R_{load1}$ and $R_{load2}$. At $t$ = 160ms, the fault condition is detected, as indicated by a fault flag (F) = 1 (dark blue curve). The converter starts operating at the lower current limit ($I_{dc\_lcl}$ = 2A) but the emulated DER remains supplying 5A, the set current limit of the DC power supply. It takes about 20ms for contactors K2 and K3 to open isolating the faulted segment/node, as indicated by $I_{cs2} = 0A$ and $I_{cs3} = 0A$. After fault isolation, the system returns to normal operation (droop control), $V_{dc}$ increases to 47.6V in both nodes. $R_{load1}$ is fed by the "emulated DER" and $R_{load3}$ by the 4-switch converter.

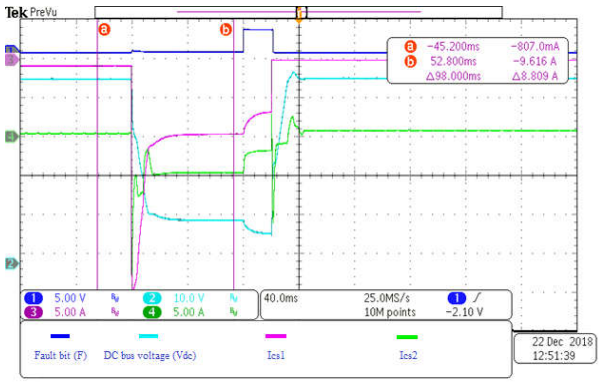



Fig. 9. Fault occurs at node 'A'. *Ch*1 (dark blue): *Fault bit* (*F*); *Ch*2 (light blue): *DC bus voltage at converter* ($V_{dc}$); *Ch*3 (pink): *current in sensor CS*1 ($I_{cs1}$); *Ch*4 (green): *current in sensor CS*2 ($I_{cs2}$).

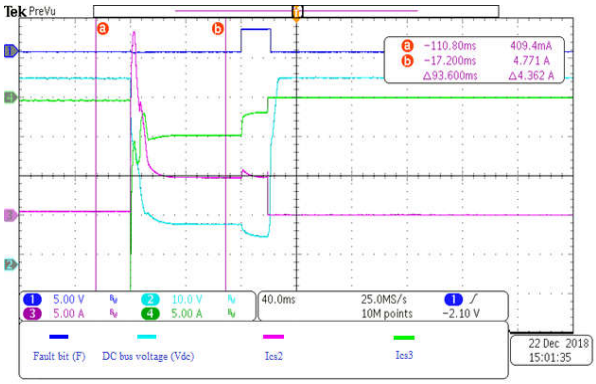



Fig. 10. Fault occurs at node 'B'. *Ch*1 (dark blue): *Fault bit (F)*; *Ch*2 (light blue): *DC bus voltage at converter* ($V_{dc}$); *Ch*3 (pink): *current in sensor CS*2 ($I_{cs2}$); *Ch*4 (green): *current in sensor CS*3 ($I_{cs3}$).

*When a fault occurs at node 'C'*

The main waveforms of the system when a fault occurs at node 'C' are shown in Fig. 11. This case is similar to when the fault occurs at node 'A'. As in the previous cases, the system is initially operating in the normal mode. The DC bus voltage $V_{dc}$ (light blue curve) is 47.4 V, and the current flowing near the faulted node, current sensors $I_{cs3}$ (pink curve) is -400mA and $I_{cs4}$ (green curve) is 794mA. At $t$ = 80ms, a 1.1Ω fault impedance is connected to node 'C'. Following a short transient, $V_{dc}$ decreases to 10.5V, with both DERs operating at maximum current limit (5A). $I_{cs3}$ increases to 4.6A and $I_{cs4}$ increases to 9.6A. Although each DER is in maximum current limit mode i.e. 5A, not all the current is flowing to the connected fault resistance ($R_{fault}$) of 1.1Ω at bus 'C'. Some current still flows to $R_{load1}$ and $R_{load2}$. At $t$ = 160ms, the fault condition is detected as indicated by a fault flag (F) = 1 (dark blue curve). The converter starts operating at $I_{dc\_lcl}$ = 2A while the emulated DER remains supplying 5A. This lasts for 20 ms, until contactor K4 opens and isolates the faulted segment. After

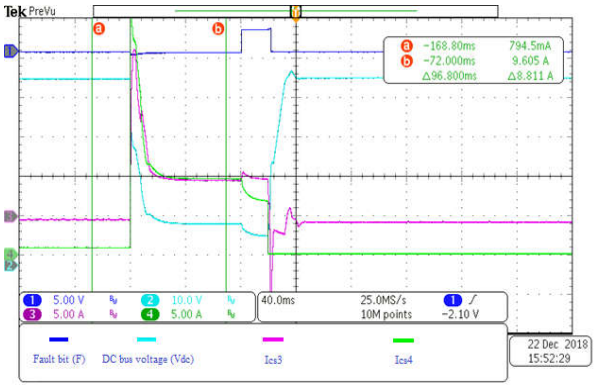



Fig. 11. Fault occurs at node 'C'. *Ch*1 (dark blue): *Fault bit* (*F*); *Ch*2 (light blue): *DC bus voltage at converter* ($V_{dc}$); *Ch*3 (pink): *current in sensor CS*3 ($I_{cs3}$); *Ch*4 (green): *current in sensor CS*4 ($I_{cs4}$)

fault isolation, the system returns to normal operation (droop control), $V_{dc}$ increases to 47.6V, $I_{cs3} = -800mA$ and $I_{cs4} = 0A$ and loads 1 and 2 are fed by the two DERs.

## VI. CONCLUSION

In this paper, the implementation of a fault protection scheme for a DC nanogrid with distributed energy resources (DERs) based on the coordination of a fault-insensitive converter and low-cost contactors is presented. The location of the faulted segment(s) is identified by means of peer-to-peer communication between neighboring DERs. In this work, this was implemented with Controller Area Network (CAN) communication. This method requires a fault-insensitive power electronics interface capable of reducing the injected currents, so that the low cost/current contactors can open safely. A laboratory set-up was built to verify the effectiveness of the developed protection scheme for a DC nanogrid with multiple droop-controlled DERs. Experimental results shown that the developed protection scheme was able to identify a fault and its location and isolate/disconnect only the faulted segment, protecting the entire system from shutdown.

## REFERENCES


[1] S. K. Kollimalla, M. K. Mishra and N. L. Narasamma, "Design and Analysis of Novel Control Strategy for Battery and Supercapacitor Storage System," *IEEE Transactions on Sustainable Energy*, vol. 5, no. 4, pp. 1137-1144, Oct. 2014.

[2] D. Wang, A. Emhemed, P. Norman and G. Burt, "Evaluation of Existing DC Protection Solutions on an Active LVDC Distribution Network under Different Fault Conditions," *CIRED – Open Access Proceeding Journal*, vol. 1, no. 1, pp. 1112-1116, Jun. 2017.

[3] A. Emhemed, K. Fong, S. Fletcher and G. Burt, "Validation of Fast and Selective Protection Scheme for an LVDC Distribution Network," *IEEE Transactions on Power Delivery*, vol. 32, no. 3, pp. 1432-1440, Jun. 2017.

[4] A. Meghwani, S. Srivastava and S. Chakrabarti, "A Non-Unit Protection Scheme for DC Microgrid Based on Local Measurements," *IEEE Transactions on Power Delivery*, vol. 32, no. 1, p. 172–181, 2016.

[5] J. Ma, J. Li and Z. Wang, "An adaptive distance protection scheme for distribution system with distributed generation," *5th International Conference on Critical Infrastructure* (CRIS), Beijing, 2010.

[6] K. Jia, T. Bi, B. Liu, E. Christopher and D. W. P. Thomas and M. Sumner, "Marine Power Distribution System Fault Location Using a Portable Injection Unit," *IEEE Transactions on Power Deliv*ery, vol. 30, no. 2, p. 818–826, 2015.

[7] J.-D. Park, J. Candelaria, L. Ma and K. Dunn, "DC Ring-Bus Microgrid Fault Protection and Identification of Fault Location," *IEEE Transactions on Power Delivery*, vol. 28, no. 4, pp. 2574-2584, Oct. 2013.

[8] M. Hajian,D. Jovcic and B. Wu, "Evaluation of Semiconductor Based Methods for Fault Isolation on High Voltage DC Grids," *IEEE Transactions on Smart Grid*, vol. 4, no. 2, pp. 1171-1179, Jun. 2013.

[9] J. Schönberger, R. Duke and S.D. Round, "DC-bus signaling: A distributed control strategy for a hybrid renewable nanogrid," *IEEE Transactions on Industrial Electronics*, vol. 53, pp. 1453-1460, 2006.

[10] A. Choubey and L. A. C. Lopes, "A Tri-state 4-switch Bi-directional Converter for Interfacing Supercapacitors to DC Micro-grids", in IEEE 8th International Symposium on Power Electronics for Distributed Generation Systems, Florianopolis, Brazil, April 17-20, 2017.

[11] S. Saeed, "Fault Protection Scheme for DC Nanogrids Based on the Coordination of Fault-Insensitive Power Electronic Interfaces and Contactors", M.A.Sc. Thesis, Electrical & Computer Engineering Department, Concordia University, Montreal, QC, 2019.