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Power consumption analysis of MOSFET and Single electron transistor for inverter circuit

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ABSTRACT

This paper represents performance of analysis of low power consumption in single electron transistor (SET) for inverter circuit. Rather than MOSFET Single Electron Transistor that may be used as a voltage-controlled switch. Current flowing through the SET is result of the electron tunnelling through the tunnel junctions. Therefore, the demand for supply voltage is also very low. As a result, power consumption on the SET is much lower as compare to MOSFET. The SET is a low power device is used to produce new features, which is almost impossible to achieve in the CMOS region. In this simulation the research work was done through MATLAB with an inverter built by SETs and MOSFETs.

Selection and peer-review under responsibility of the scientific committee of the International Conference on Advances in Design, Materials and Manufacturing.

1. Introduction

The Power consumption and thermal problems are now central to the construction in the Electronic system. For applications with high performance, heat affects integration density, efficiency reliability, power consumption and cost. In battery-powered systems power consumption directly determines the life time of the system. Power consumption problems are solved by the new technologies that increased energy per operation, allowing for density increases and ultimately performance. Energy and thermal problems were some of the major reasons for replacing vacuum tubes through semiconductor devices in the 1960 s and replacing BJT through CMOS in the 1990 s. CMOS is a standard design technology used today. As the integrated circuit (IC) integration increases, it will reach power consumption, thermal limits, and fabrication; it may be time for another switch to a very different technology [1].

The scaling of a MOSFET is important to reduce power loss throughout the device. The developments of CMOS technology have been made by the engineers for almost 30 years according to Moore's law. Some researchers have advice that CMOS may not be scaled down in upcoming years. The International Technology Road map for Semiconductors (ITRS) has determined the size of integrated circuits for the next a number of years in terms of the Moore's Law (Fig. 1 Fig. 2).

MOSFET is considered to be a main element of the ITRS system. According to ITRS the existing computing hardware are based on the '22 nm ' technology node. It means that the feature size (gate length) of the standard MOSFET is 22 nm. ITRS has a road map where 14 nm, 10 nm and 7 nm technology node will be successor to 22 nm technology node follower in a year 2014, 2016 and 2018 respectively. An MOSFET can support only up to 11 nm technology. Therefore, the small MOSFET feature size does not support 10 nm nodes and 7 nm technology nodes. It is therefore clearly understood that CMOS technology is gradually invalid in future. So reduce the power dissipation at each MOSFET gate will no longer be possible. To ensure continuous improvement in this area new switching devices must be used [2].

The single electron transistor is a nano device, offers exceptional potential for coming Ultra Large Scale Integrated (ULSI) circuits because of its size scale integration and low power consumption. SET is a four-terminal device, it has a source and drain along with two separate gates. First gate has the same functionality as a CMOS transistor gate and the other gate is specially used as a back gate is used for controlling purpose.

A SET has a small island that attached with source and drain is led by tunnel junctions, and is capacitively connected with one or

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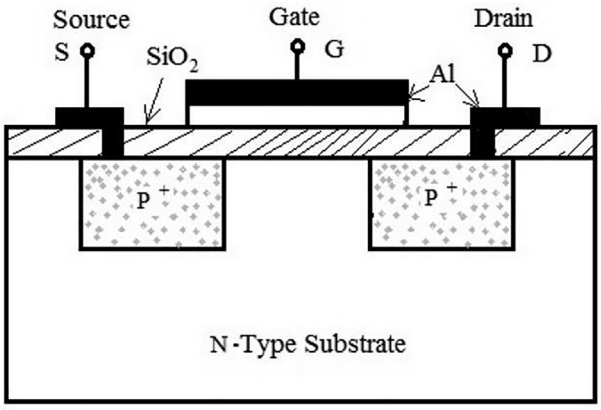

Fig. 1. Operation of enhancement PMOS.

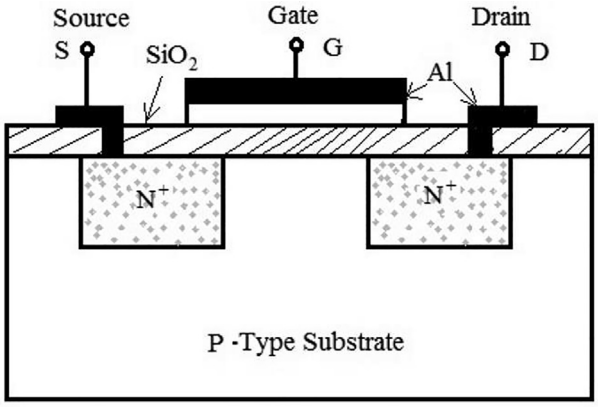

Fig. 2. Operation of enhancement NMOS.

more gates [3]. The Single Electron Transistor can act as a voltage biased switch witch turn on when the tunnelling current flows through it and then turn off when the current cannot flow through it. According to the rules of classical physics, current can't pass through a capacitor if the capacitor is connected directly to the constant voltage source. But according to quantum physics, however, there is a non-vanishing probability for an electron will pass through a thin insulating barrier or a thin capacitor. This process is well-known as Quantum tunnelling [4,5]. The level of the current flow due to tunnelling of electron is very low. So tunnelling current is very low (in nanoampere). Therefore, supply voltage requirement of SET-based digital circuits is also very low (usually in millivolt). In addition, the SET has the advantage of being smaller in size (size of quantum dots are a few nanometres). So, because of above reason SET is a better replacement of MOSFET.

2. Basic theory of MOSFET

There are two type of enhancement-MOSFET

(a) P-channel MOSFET

In the enhancement type PMOS threshold voltage V_T, (at Zero body bias) it is considered negative, the current I_{SD} flows from the source to the drain and μ_p is the mobility of a hole.

In the p-channel MOSFET the equation of different region is expressed as:

In Cut off ($V_{SG} \leq |V_T|$),

$$I_{SD} = 0 \tag{1}$$

In Linear ($V_{SG} > |V_T|$, $V_{SD} \leq V_{SG}-|V_T|$),

$$I_{SD} = \mu_P C_{OX} \frac{W}{L}\left[(V_{SD} - |V_T|)V_{SD} - \frac{V_{SD}^2}{2}\right] \tag{2}$$

In Saturation ($V_{SG} > |V_T|$, $V_{SD} > V_{SG} - |V_T|$),

$$I_{SD} = \frac{1}{2}\mu_P C_{OX} \frac{W}{L}(V_{SG} - |V_T|)^2 \tag{3}$$

(b) n-channel MOSFET

In the enhancement type NMOS threshold voltage V_T, (at Zero body bias) it is considered positive [6], the current I_{DS} flows from the drain to the source and μ_n is the mobility of an electron.

In the n-channel MOSFET the equation of different region is expressed as:

In Cut off ($V_{GS} \leq V_T$),

$$I_{DS} = 0 \tag{4}$$

In Linear ($V_{GS} > V_T$, $V_{DS} \leq V_{GS} - V_T$),

$$I_{DS} = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - |V_T|)V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{5}$$

In Saturation ($V_{GS} > V_T$, $V_{DS} > V_{GS} - V_T$),

$$I_{DS} = \frac{1}{2}\mu_n \mathrm{Cox} \frac{W}{L}(V_{GS} - V_T)^2 \tag{6}$$

3. Basic theory of Single electron transistor

Every SET has three terminals and one island, these are source, drain and gate. Insulating tunnel junctions is between drain- island & source - island. The gate - island is a gate capacitor. By applying various voltages on gate of tunneling electron through tunnel junctions may be controlled [7]. Fig. 3 shows the Single Electron Transistor.

For the purpose of appropriate switching one more gate has been introduced. The gates are coupled with island with capacitors C_{g1} and C_{g2} respectively. A Source and drain are joined to the island by two - tunnel junctions. These two-tunnel junctions have very low capacitive impedance C_1 and C_2 respectively. There is one point to keep in mind that current flow is caused by the tunneling of electrons through two tunnel junctions. Fig. 4 shows the equivalent SET circuit [8]. The Output stray capacitor C_0 and background charger Q_0 is shown in circuit model. The SET is highly sensitive to background charging.

Voltage of the island V (which is function of n), ne (charge present is the island) then,

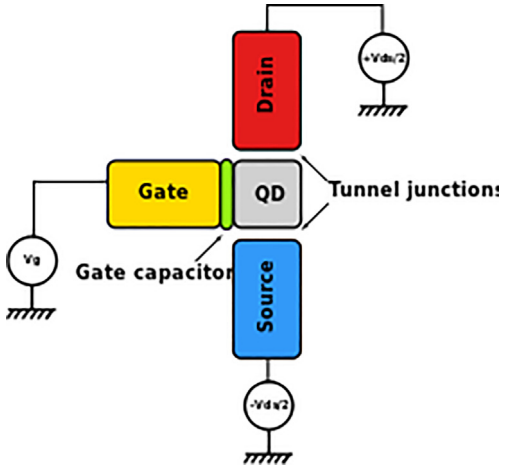

Fig. 3. Single electron transistor.

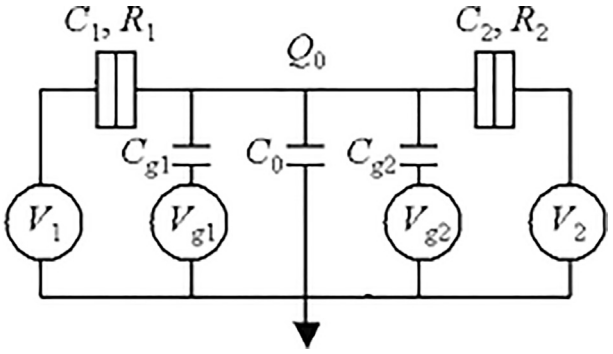

Fig. 4. Single electron transistor - scheme diagram.

$$V(n) = \frac{ne + V_1C_1 + V_2C_2 + V_{g1}C_{g1} + V_{g2}C_{g2} + Q_0}{C_{\sum}} \quad (7)$$

Here, $C_{\sum}$= C_1 + C_2 + C_{g1} + C_{g2} + C_0

The change of energy due to tunneling of a charge e of island isΔE_i,

$$\Delta E_i = -eV_i + eV(n) + \frac{e^2}{2C_{\sum}} \quad (8)$$

Here, amount of electrostatic energy = eV(n) + $\frac{e^2}{2C_{\sum}}$and voltage of lead = V_i

Now rate of tunneling Γ_i can be given as.

$$\Gamma i = \frac{\Delta E_i}{e^2R_i(\frac{\Delta E_i}{k_BT} - 1)} \quad (9)$$

Where, R_i = Tunnel resistance, k_B = Boltzmann constant, and T = Absolute temperature

There are four possible ways of tunneling of charge as given, Γ_{R1}, Γ_{R2} is the tunneling through tunnel junction 1 and 2 respectively in the direction of right, Γ_{L1}, Γ_{L2} is the tunneling through tunnel junction 1 and 2 respectively in the direction of left, Co-tunneling is ignored here [9].

Then probabilities of the charge states

$$P(n) = P(n-1)(\frac{\Gamma_{L2}(n-1) + \Gamma_{R1}(n-1)}{\Gamma_{R2}(n) + \Gamma_{L1}(n)}) \quad (10)$$

The average current from tunnel junction 1 to 2,

$$I = \sum_n eP(n)(\Gamma_{R1}(n) - \Gamma_{L1}(n)) \quad (11)$$

Then islands average voltage

$$V = \sum_n V(n)P(n) \quad (12)$$

Charge state n should be calculated with the highest possibility.

$$n_{opt} = \frac{Q_0 + V_1C_1 + V_2C_2 + V_{g1}C_{g1} + V_{g2}C_{g2}}{e} + \frac{C_{\sum}}{e} \times \frac{R_2V_1 + R_1V_2}{R_1 + R_2} \quad (13)$$

The basic functionality of a single electron transistor can be found and all of these equations implemented using the conventional hypothesis of electron tunneling in SET [10].

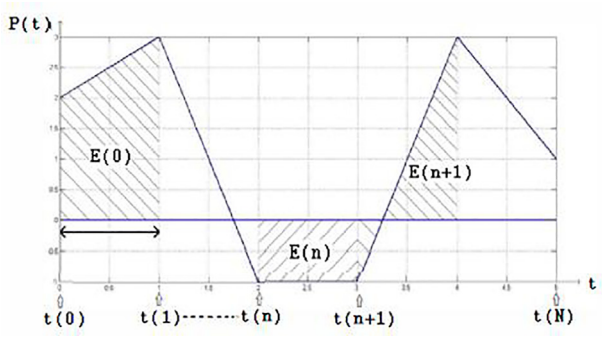

Fig. 5. Average power calculation method.

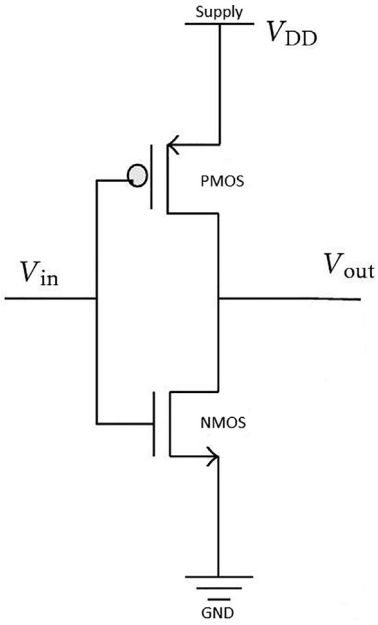

Fig. 6. CMOS inverter.

4. Calculate average power consumption and the simple digital circuit - an inverter

Fig. 5 shows time - power dissipation curve. In this graph area E (0) refers to the energy dissipated for the time period t (1) – t (0), this area is covered by the power dissipation curve like time axis and the perpendiculars points between two curve boundaries [11]. Sometimes this area can be trapezoidal like E (0), sometimes rectangular like E (n) or sometimes a combination of two triangles like E (n + 1). Therefore, the energy dissipated in graph

$$E = \sum_{n=0}^{N-1} E(n) \quad (14)$$

Now, we can calculate the average power dissipation for time period, T = t (N)−t (0) by P = $\frac{E}{T}$

In Fig. 6 shows the CMOS inverter, in this the PMOS and NMOS makes the circuit of CMOS inverter and in Fig. 7 shows the SET inverter circuit, in this above PSET island is black. This means that background charge is negative. The blow NSET island is white. The tariff mark on the back of the both islands is contradictory but their total values are assumed to be equal. The explanation of the background charges and characteristics of the SET inverter and CMOS inverter [12].

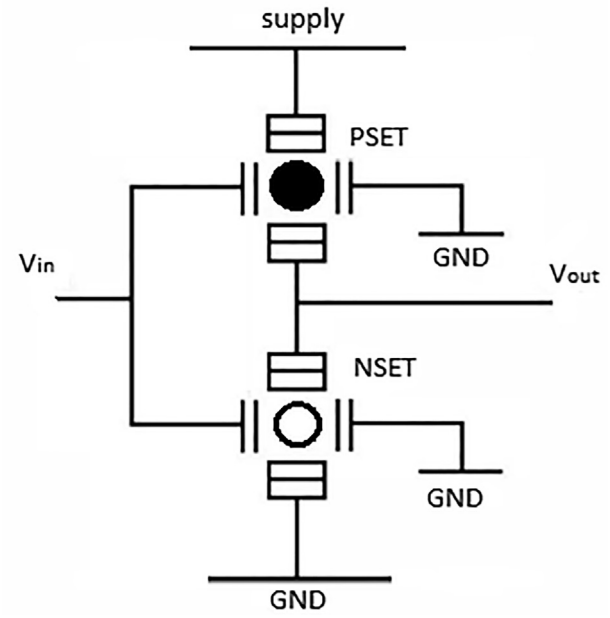

Fig. 7. SET based inverter.

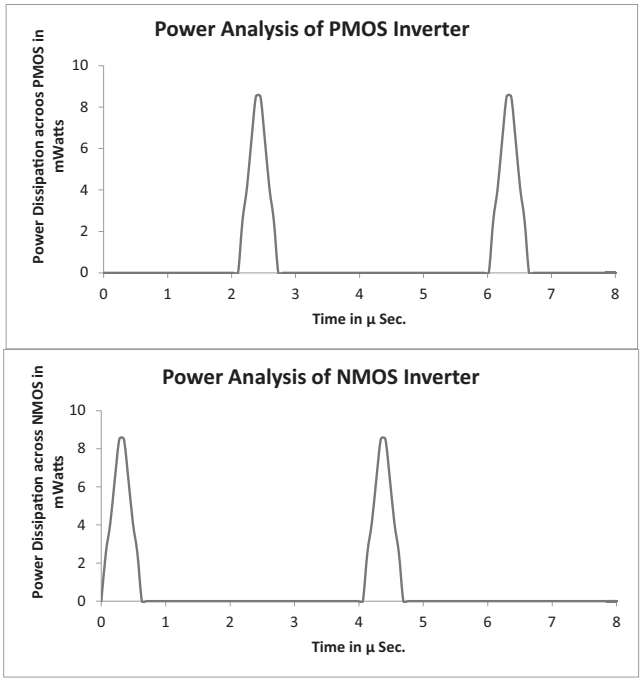

Fig. 8. Power consumption analysis for the PMOS and NMOS of a CMOS inverter.

5. Comparisons between CMOS inverter and SET based inverter

Power consumption curves in the PMOS & NMOS CMOS inverter circuits are shown in Fig. 8 and the power consumption curves in the PSET & NSET SET-based inverter circuit are shown in Fig. 9.

Now taking a power consumption values for different time average power consumption have been calculated by MATLAB for both CMOS inverter and SET based inverter circuits using the above-mentioned power consumption method. By the simulation following results were found.

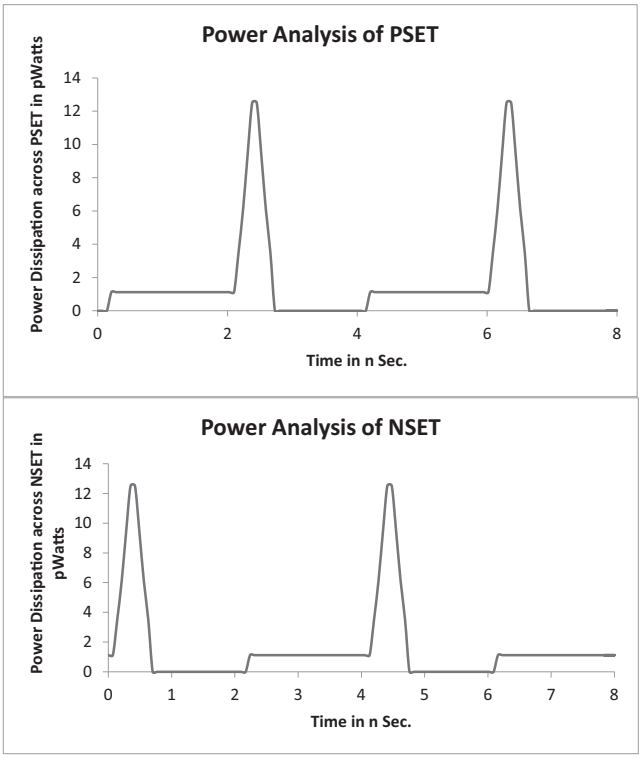

Fig. 9. Power consumption analysis for the PSET and NSET of a SET based inverter.

CMOS inverter average power dissipation for the PMOS is 3.3708×10^{-5} Watt and for the NMOS is 3.1701×10^{-5} Watt. Hence total average power dissipation across the CMOS inverter is 6.5409×10^{-5} Watt.

Now for the SET based-inverter average power dissipation for PSET is 6.6061×10^{-12} Watt and for NSET is 6.7223×10^{-12} Watt. Hence total average power dissipation across the SET based inverter is 13.3284×10^{-12} Watt.

6. Results and conclusion

Power analysis shows same results for both CMOS inverter and SET-based inverter. Simulation results clearly show that total power consumption of SET-based inverter is many times lesser amount of CMOS inverter. This model is designed to look at the conventional hypothesis where co-tunnelling is neglected. With the most valuable results we can consider. We have a lot of expertise in terms of SET-based technology. SET is a future device that makes the integration technology to be reached the new level of technology. The SET will be play important role for nanoelectronics applications.

CRediT authorship contribution statement

Brijendra Mishra: Investigation, Methodology, Project administration, Resources, Software, Validation, Visualization, Writing - original draft, Writing - review & editing. **Vivek Singh Kushwah:** Investigation, Methodology, Project administration, Resources, Software, Validation, Visualization, Writing - original draft, Writing - review & editing. **Rishi Sharma:** Investigation, Methodology, Project administration, Resources, Software, Validation, Visualization, Writing - original draft, Writing - review & editing.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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