Ultrahigh Voltage Gain DC-DC Boost Converter with ZVS Switching Realization and Coupled Inductor Extendable Voltage Multiplier Cell Techniques

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***Abstract*— In this paper, a novel ultrahigh voltage gain dc-dc boost converter with expandable diode-capacitor voltage multiplier (VM) cells is presented. The diode-capacitor VM cells and coupled inductors are employed in the presented topology to provide a higher voltage gain. Also, the main and the auxiliary power switches of the presented converter operate with zero voltage switching (ZVS). The coupled inductors' leakage inductances control the rates of the current drop in the voltage multiplier diodes, which decreases their reverse recovery losses markedly. Moreover, the voltage stresses on all capacitors and semiconductors are reduced significantly. In this converter, the number of voltage multiplier cells, and the coupled inductors turn ratios provide three degrees of design freedom. These degrees of freedom are used to set the desired voltage stresses of the semiconductors within the desired range and to provide a high voltage gain at optimum duty cycles. The design and theoretical analysis of the presented converter are discussed. Finally, the performance of the presented converter is validated using a 500 W, 40 V/380 V laboratory prototype converter, and the experimental results confirm the theoretical calculation.**

***Index Terms*— Coupled inductor, diode-capacitor voltage multiplier cells, ultrahigh step-up dc-dc converters, zero voltage switching.**

I. Introduction

NOWADAYS, designing and implementing the efficient dc/dc converters have attracted significant attention. These converters are implemented to convert a dc input voltage to a desired output voltage. Buck and Boost converters are the most well-known types of dc-dc converters which are used to decrease and increase the dc voltage levels, respectively. [1]-[3]. In the case of Boost converters, due to the lower level of the input voltages in the required applications, high voltage gain capability is required [4]. To achieve a high voltage-gain, the duty cycle must be set to be significantly high in the conventional boost converters, which can lead to high power loss. Hence, the use of high step-up dc-dc structures to produce a high voltage range with a lower duty cycle is a great solution for these applications [5]-[6].

Various techniques to raise the voltage gain of the dc-dc converters were presented in the reported literature, such as the use of coupled inductors, transformers, and voltage multiplier modules [7]-[8]. The most important characteristics for a desired topology are the cost, size, and efficiency. In general, the use of many passive elements in the high voltage gain topology not only increases the cost but also reduces the efficiency of the topology [9]-[10]. By increasing the switching frequency in the dc-dc converters, the cost and the size can be reduced. However, the high switching frequencies may cause high switching losses [11]. Thus, many other converter topologies were introduced as optimal topologies in terms of cost, size, and losses. The main losses of the dc-dc converters are due to the losses in the power switches and power diodes due to reverse recovery losses [12]. Thus, hard switching operation should be avoided to ensure lower converter losses [13]-[19].

To reduce the switching losses and the reverse recovery issues of the diodes, three main types of soft-switching, operations are usually used, (i) zero voltage switching (ZVS), (ii) zero current switching (ZCS), and (iii) zero voltage zero current switching (ZVZCS) conditions.

By turning on the power switches and turning off the power diodes under ZCS, the switching losses and reverse recovery issues of the diodes in [20]-[21] are eliminated. Furthermore, by combining coupled inductors and VM cells, not only a high voltage-gain but also low voltage stress across the power semiconductor switching devices can be obtained. Because of the many elements needed in such converter topologies, the topologies face increased control complexity, cost, and a spike in turn-off losses. Various topologies to obtain high voltage gains and ZVS capabilities have been proposed in [22]-[28]. In [24]-[25], the power switches are turned on with soft-switching and the diodes are turned off with zero currents, which eliminates the reverse recovery issues. In [24], it was reported that the number of power switches and the voltage stresses across the voltage multiplier capacitors are high. Furthermore, in [25], it was reported that not only the number of power switches is high, but also the design and implementation of the coupled inductors are complicated. These disadvantages raise the volume, expense, and complexity of the topologies.

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In this paper, a new ultra-high step-up dc-dc converter with expandable diode-capacitor VM cells is proposed. The main contributions of the proposed converter are:

- Ultrahigh voltage gain and soft-switching performance can be achieved with a minimum number of power switches and elements compared with other converters with the same function.
- The voltage stress across all the capacitors is minimum. This feature reduces the cost and volume of the converter significantly.
- The clamped capacitors are used in a technique to clamp the voltage stress across the diodes and switches and increase the converter voltage gain.
- The size of the second coupled inductor is small. Also, it is used not only to raise the converter voltage gain but also to produce the ZVS performance for the power switches.

As a result, in this structure, the number of elements is reduced, resulting in the reduced volume, cost, and complexity of the converter. Therefore, based on these features, the converter is a good candidate for Boost converters to provide a high voltage gain with an optimum number of components.

II. Proposed Extendable Ultra-High Step-Up DC-DC Converter

The topology of the proposed ultra-high step-up dc-dc converter with expandable diode-capacitor voltage multiplier cells is shown in Fig. 1. This figure shows that the proposed topology consists of two coupled inductors, one main switch, an auxiliary switch, and several VM cells made up of capacitors, and diodes. In Fig. 1, V_{in}, V_{out}, and R_{out} indicate the voltage of the input source, the voltage of the output load, and the load resistance, respectively. Also, D_1 and D_2 are the boost diodes. The diodes and the capacitors of the M_{th} stage of the diode-capacitor VM cells are $D_{VM(2M-1)}$, $D_{VM(2M)}$, and $C_{VM(2M-1)}$, $C_{VM(2M)}$, respectively. The main and auxiliary switches are S and S_{AUX}, respectively, and the snubber capacitor of the main switch, S, is C_S. Also, C_{C1} and C_{C2} are the clamped capacitors of the converter. Fig. 1 shows that the turn ratios of the coupled inductors are $n = n_s/n_p$ and $N = N_S/N_P$. L_{LK1}, L_{LK2}, and L_{m1}, L_{m2} are the leakage inductances and the magnetic inductances of the coupled inductors, respectively.

In this paper, to analyze and describe the proposed ultra-high step-up dc-dc converter easily, one stage of the diode-capacitor VM cells is chosen. Figs. 2 and 3 show the eight operational modes of the proposed topology and their key waveforms, respectively.

***Mode* I [t_0 - t_1]:** The main switch S, and the auxiliary switch S_{AUX} are off at t_0. However, in this mode, the current of L_{LK1} (i_{LK1}) has a positive value and a negative current flows through L_{LK2} (i_{LK2}). The summation of i_{LK1} and i_{LK2} is negative, thus switch S and the anti-parallel diode of S (D_S) conduct a negative current. Thus, the relationship related to this mode is given as follows:

$$i_{LK1} > 0,\ i_{LK2} < 0,\ |i_{LK2}| > |i_{LK1}|,\ \ i_S = (i_{LK1} + i_{LK2}) < 0 \qquad (1)$$

In the diode-capacitor cells, D_{VM1} and D_{VM2} are in the off-state and on-state, respectively.

***Mode* II [t_1 - t_2]**: Diode D_{VM1} starts conducting while diode D_{VM2} turns off at t_1. Thus, the capacitor, C_{VM1}, is charged via the current of the coupled inductors' secondary side, and the capacitor, C_{VM2}, is discharged into the load (R_{out}). Also, in this mode, the magnetic and leakage inductances are charged.

***Mode* III [t_2 - t_3]**: Like the previous mode of operation, the capacitors, C_{VM1}, and C_{VM2}, in the diode-capacitor cells are charged and discharged, respectively. Also, the negative current through the main switch S reaches zero at t_2, which leads to the switch turn-on under ZVS. The following equations express the voltage and current of the coupled inductors:

$$V_{Lm1} = \left[L_{m1}/\left(L_{LK1} + L_{m1}\right)\right]V_{in} \qquad (2)$$

$$V_{Lm2} = \left[L_{m2}/\left(L_{LK2} + L_{m2}\right)\right]V_{Cc1} \qquad (3)$$

$$i_{Lm1}(t) = i_{Lm1}(t_2) + \left(L_{m1}V_{in}/\left(L_{LK1} + L_{m1}\right)\right)(t - t_2) \qquad (4)$$

$$i_{Lm2}(t) = i_{Lm2}(t_2) + \left(L_{m2}V_{Cc1}/\left(L_{LK2} + L_{m2}\right)\right)(t - t_2) \qquad (5)$$

$$i_{LK1}(t) = i_{Lm1}(t) + ni_{DVM1}(t) = i_{LK1}(t_2) + \left(L_{LK1}V_{Cc2}/\left(L_{LK1} + L_{m1}\right)\right)(t - t_2) \qquad (6)$$

$$i_{LK2}(t) = i_{Lm2}(t) + Ni_{DVM1}(t) = i_{LK2}(t_2) + \left(L_{K2}V_{Cc2}/\left(L_{LK2} + L_{m2}\right)\right)(t - t_2) \qquad (7)$$

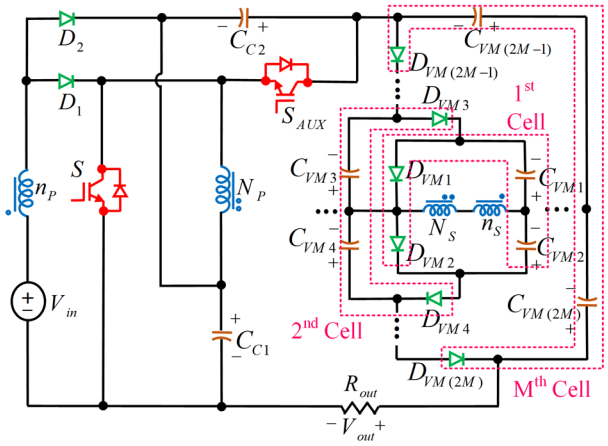


Fig. 1. The presented ultrahigh step-up dc-dc converter with expandable diode-capacitor VM cells.

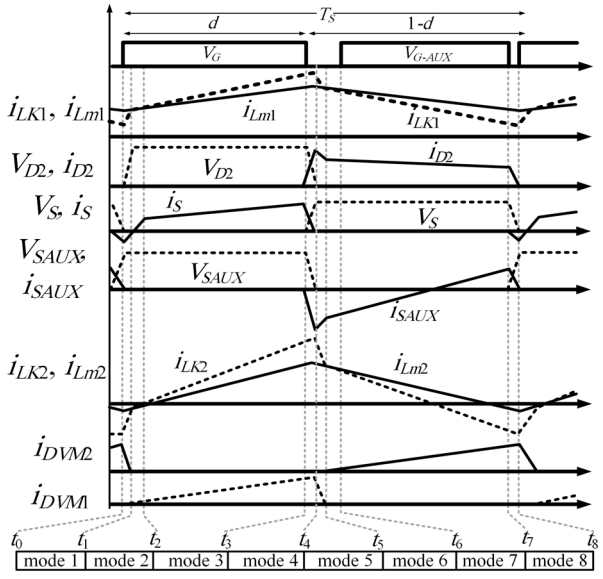


Fig. 2. Key waveforms of the presented topology.

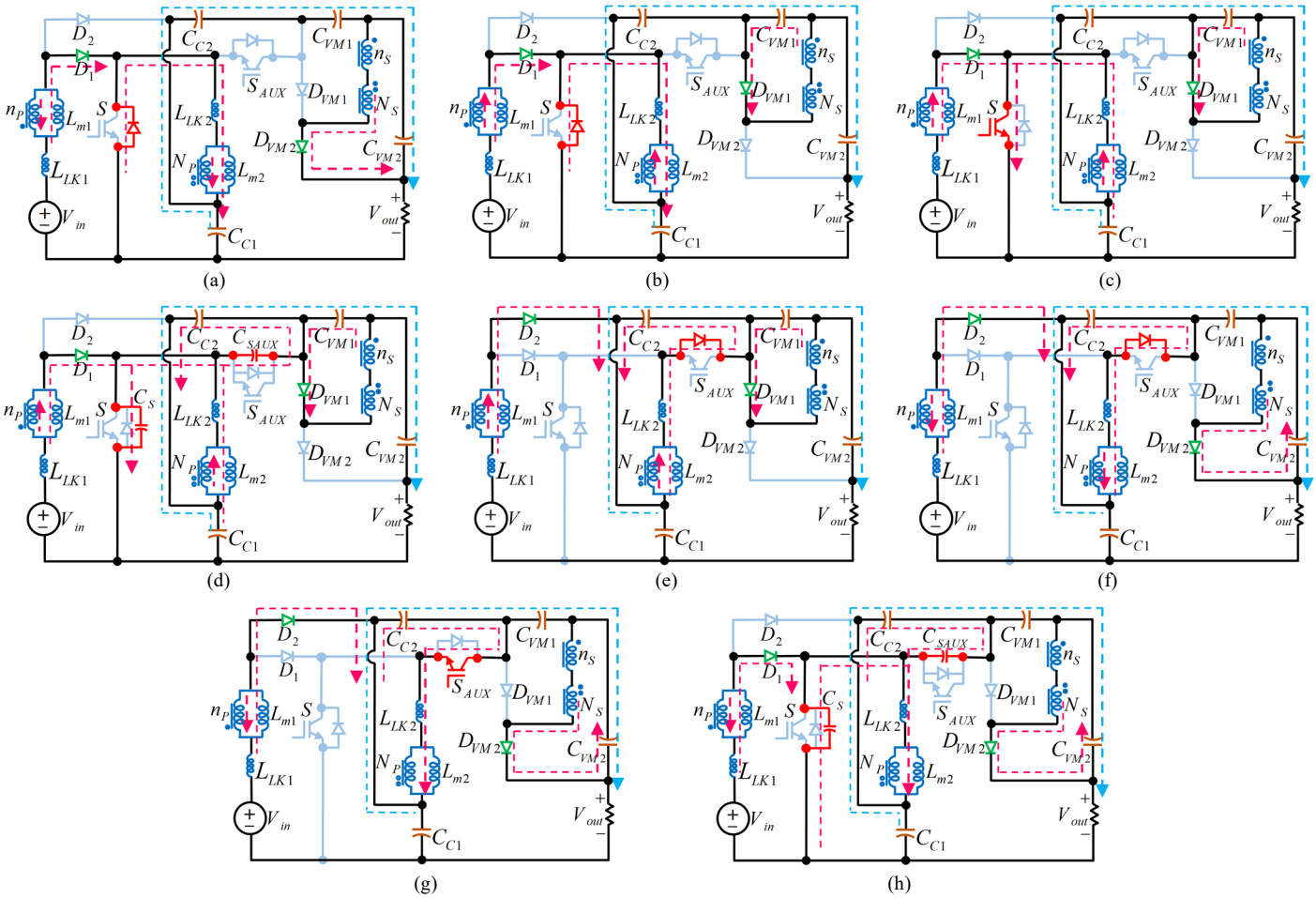


Fig. 3. The proposed converter in various operational modes: (a) mode I, (b) mode II, (c) mode III, (d) mode IV, (e) mode V, (f) mode VI, (g) mode VII, and (h) mode VIII.

***Mode* IV [t_3 - t_4]:** By turning off switch S at t_3, the current i_{LK2} charges the snubber capacitor of the main switch (C_S) to (V_{Cc1}+ V_{Cc2}). Also, it discharges the snubber capacitor of the auxiliary switch (C_{SAUX}) from (V_{Cc1}+ V_{Cc2}) to zero. The voltage across switch S increases because of the charging of the snubber capacitor C_S. Thus, the main switch turns off with a lower current and voltage, which provides near to soft turn-off. Because of the short duration of this mode (t_3 - t_4), the currents are assumed to be constant, which is given in (8):

$$t_{3-4} \approx C_{S1}\left[V_{Cc1}/\left(i_{LK1}(t_3)+i_{LK2}(t_3)\right)\right] \approx C_{SAUX}V_{Cc2}/i_{LK2}(t_3) \qquad (8)$$

The capacitors in the diode-capacitor VM cells have the same prior behavior.

***Mode* V [t_4 - t_5]:** At the end of mode IV, the voltage across switch S_{AUX} reaches zero, then a negative current through the auxiliary switch causes the anti-parallel diode of the auxiliary switch (D_{SAUX}) to turn on at t_4. As D_2 and D_{SAUX} conduct, the currents i_{LK1} and i_{LK2} flow through the capacitors C_{C1} and C_{C2}, respectively, charging the capacitors. The charging currents of the capacitor C_{C2} can be expressed in (9):

$$i_{LK2}(t)=i_{Cc2}(t)\approx\left(\frac{-L_{LK2}V_{Cc2}(t)}{(L_{LK2}+L_{m2})}\right)\frac{\sin(\omega_4(t-t_4))}{Z_4}+i_{LK2}(t_4)\cos(\omega_4(t-t_4)) \qquad (9)$$

where $Z_4=\sqrt{(L_{m2}+L_{LK2})/C_{C2}}$ and $\omega_4=1/\sqrt{(L_{m2}+L_{LK2})C_{C2}}$. The currents of these inductances decrease because the negative voltages drop across the leakage and the magnetizing inductances. Moreover, the leakage inductances L_{LK1} and L_{LK2} cause the secondary side current of the coupled inductors to decrease to zero current at the end of this mode. It is to be noted that L_{LK1} and L_{LK2} control the rate of current falling in the VM diodes, which solves the diodes reverse recovery problems.

***Mode* VI [t_5 - t_6]:** However, in this mode, when diode D_{VM1} turns off, diode D_{VM2} starts conducting, thus, C_{C1} and C_{C2} are charged. Also, diode D_2 continues conducting the current i_{LK1}. The auxiliary switch via the anti-parallel diode D_{SAUX} conducts the resonant loop current. Furthermore, capacitor C_{VM1} is discharged into the output load and the secondary side current of the coupled inductors charges capacitor C_{VM2}.

***Mode* VII [t_6 - t_7]:** The voltage across the S_{AUX} was stable at zero in the former mode of operation, so it can be turned on under ZVS at t_6. The diodes and capacitors of the diode-capacitor cells and the main switch are in a quasi-condition state in comparison with that in mode VI. The relationship between the coupled inductors voltage and current are given as follows

$$V_{L_{m1}} = \left[L_{m1} / \left(L_{LK1} + L_{m1} \right) \right] \left(V_{in} - V_{Cc1} \right) \quad (10)$$

$$V_{L_{m2}} = \frac{1}{N} \left(\frac{\left(V_{Cc1} - V_{in} \right) n L_{m1}}{L_{LK1} + L_{m1}} - \mathrm{V}_{C_{VM2}} \right) \quad (11)$$

$$i_{Lm1}(t) = i_{Lm1}(t_6) - \left(\frac{L_{m1} \left(V_{Cc1} - V_{in} \right)}{L_{LK1} + L_{m1}} \right) (t - t_6) \quad (12)$$

$$i_{Lm2}(t) = i_{Lm2}(t_6) - \frac{1}{N} \left(\frac{\left(V_{in} - V_{Cc1} \right) n L_{m1}}{L_{LK1} + L_{m1}} + \mathrm{V}_{C_{VM2}} \right) (t - t_6) \quad (13)$$

$$i_{LK1}(t) = i_{D1}(t) = -n i_{D_{VM2}}(t) + i_{Lm1}(t) = i_{LK1}(t_6) - \left(\frac{L_{m1} (V_{Cc1} - V_{in})}{L_{LK1} + L_{m1}} \right) (t - t_6) \quad (14)$$

$$i_{LK2}(t) = -N i_{D_{VM2}}(t) + i_{Lm2}(t) = i_{LK2}(t_6) - \left(\frac{L_{LK2} (V_{Cc2} + V_{Lm2})}{L_{LK2} + L_{m2}} \right) (t - t_6) \quad (15)$$

***Mode* VIII [t_7 - t_8]:** The auxiliary switch is turned off at t_7, and the snubber capacitor C_{SAUX} starts charging to (V_{Cc1}+ V_{Cc2}) in this mode of operation. Moreover, the parallel capacitor of the main switch starts conducting and the voltage reduces from (V_{Cc1}+ V_{Cc2}) to zero. Providing ZVS for the main switch requires extraction of enough energy from the leakage inductances, L_{LK1} and L_{LK2}, to charge the parallel capacitor of switch *S*, as expressed in (16):

$$L_{LK2} \geq \left[\left((C_S + C_{SAUX}) (V_{Cc1} + V_{Cc2})^2 + L_{LK1} i_{LK1}^2 (t_7) \right) / i_{LK2}^2 (t_7) \right] \quad (16)$$

Finally, the converter operation period is completed at the end of this operational mode.

III. Steady State Study

The following assumptions are considered in this paper: (i) short periods ((t_0-t_2), (t_4-t_6), and (t_7-t_8)) are ignored, (ii) ideal semiconductor characteristics are used, (iii) leakage inductances are ignored in the calculation, and (iv) a constant current is assumed to flow through the magnetizing inductances during switching.

A) Voltage Gain

The clamp capacitor voltage, V_{Cc1} is similar to the output voltage of the traditional boost structure, which is given by (17):

$$V_{Cc1} = V_{in} / (1 - d) \quad (17)$$

where *d* is the duty cycle of the converter. Moreover, the voltage across the clamp capacitor C_{C2} can be expressed as:

$$V_{Cc2} = d V_{in} / (1 - d)^2 \quad (18)$$

Using KVL in the third operational mode, (19) is obtained:

$$V_{C_{VM1}} = V_{C_{VM4}} - V_{C_{VM2}} = \ldots = n V_{in} + N V_{Cc1} = n V_{in} + N V_{in} / (1 - d) \quad (19)$$

Furthermore, by using KVL in mode VII, (20) is obtained:

$$V_{C_{VM2}} = V_{C_{VM3}} - V_{C_{VM1}} = \ldots = \frac{n d V_{in}}{1 - d} + N V_{Cc2} = \frac{N d V_{in}}{(1 - d)^2} + \frac{n d V_{in}}{1 - d} \quad (20)$$

According to (17) and (20), the output voltage is given by:

$$V_{out} = V_{Cc1} + V_{Cc2} + V_{C_{VM1}} + V_{C_{VM2}} = \frac{N + n(1 - d) + 1}{(1 - d)^2} V_{in} \quad (21)$$

By considering the *M*-cells of the diode-capacitor voltage multiplier cells, the voltage gain from which (22) is obtained:

$$\frac{V_{out}}{V_{in}} = \frac{1 + M \left(n(1 - d) + N \right)}{(1 - d)^2} \quad (22)$$

The impact of the leakage inductances is ignored in the previous equations. Thus, (22) indicates the ideal voltage gain. The impact of the leakage inductances can be expressed as:

$$\frac{V_{out}}{V_{in}} = \frac{M \left((1 - d) n + N \right) + 1}{(1 - d)^2 \left(1 + \frac{2 f_s}{R_{out}} (n^2 L_{LK1} + N^2 L_{LK2}) \left((\frac{M}{d})^2 + (\frac{M}{1 - d})^2 \right) \right)} \quad (23)$$

B) Design of Capacitor C_S

To achieve a near to soft turn-off for switch *S*, the snubber capacitor C_S is implemented. When the switch *S* is turned off, the snubber capacitor charges. The voltage across the switch rises slightly, and the switch turns off under near to zero voltage switching. According to the various operational modes presented in Section II, the summation of the currents i_{LK1} and i_{LK2} flows to C_S. Regarding the turn-off delay time $t_{d(OFF)}$ of the main switch from its datasheet, an equation can be obtained for the snubber capacitor C_S as given in (24):

$$C_S \geq \left(t_{d(OFF)} / (V_{Cc1} + V_{Cc2}) \right) \left[i_{LK1}(t_3) + i_{LK2}(t_3) \right] \Big|_{I_{out-\max}} \quad (24)$$

where I_{out} is the output current.

C) Coupled Inductors Design

The average current in the proposed converter, which passes through the magnetizing inductance L_{m1} can be calculated as:

$$I_{Lm1} = \frac{1 + M \left(N + (1 - d) n \right)}{(1 - d)^2} I_{out} \quad (25)$$

The magnetizing inductance current ripple ΔI_{Lm1} is given by:

$$\Delta I_{Lm1} = d V_{in} / L_{m1} f_s \quad (26)$$

where f_s is the switching frequency.

To provide continuous conduction mode (CCM) for the input current, the average value of the current passes through the inductance L_{m1} should be greater than half of the ripple of its current and can be expressed as:

$$L_{m1} \geq \left(\frac{(1 - d)^2}{1 + M \left(n(1 - d) + N \right)} \right)^2 \frac{d R_{out}}{f_s} \quad (27)$$

Also, the average current passes through L_{m2} can be calculated by (28):

$$I_{Lm2} = \frac{M (N + (1 - d) n) + d}{(1 - d)} I_{out} \quad (28)$$

Also, the current ripple of L_{m2} is given by (29):

$$\Delta I_{Lm2} = \frac{V_{in} d}{L_{m2} (1 - d) f_s} \quad (29)$$

In modes I, II, and VII, the addition of the currents i_{Lm1} and i_{Lm2} should be negative to achieve soft-switching turn-on condition for switch *S,* and finally, (30) is obtained:

$$L_{m2} < \frac{d V_{in}}{2 f_s (I_{Lm1} - \frac{\Delta I_{Lm1}}{2} + I_{Lm2} - \frac{M (n + N)}{(1 - d)} I_{out})(1 - d)} \quad (30)$$

It should be noted that the worst conditions for providing ZVS are the maximum working duty cycle and full-load conditions. Therefore, to guarantee soft-switching conditions, the value of L_{m2} should be designed for maximum working duty cycle and

full-load condition. Thus, it can be noted that by designing in the mentioned conditions, ZVS is achievable in all lower output powers and duty cycles, even at the minimum output power (0.1 full-load) and duty cycle.

D) Voltage and Current Stresses

The voltage stress on diode D_2 is equal to the clamp capacitor C_{C1} voltage. According to (17) and (22), the drop in the voltage stress of this component is expressed as (31):

$$V_{D2}=\frac{V_{in}}{1-d}=\frac{V_{out}(1-d)}{1+M\left(N+n(1-d)\right)} \tag{31}$$

Also, the voltage stress on diode D_1 is equal to the clamp capacitor C_{C2} voltage. By using (17) and (22), the voltage stress on diode D_1 can be obtained as (32):

$$V_{D1}=V_{Cc2}=\frac{dV_{in}}{(1-d)^2}==\frac{dV_{out}}{1+M\left(n(1-d)+N\right)} \tag{32}$$

The voltage stresses on the main and auxiliary switches are equal, which are given by:

$$V_S=V_{SAUX}=V_{Cc1}+V_{Cc2}=\frac{V_{in}}{(1-d)^2}=\frac{V_{out}}{M\left((1-d)n+N\right)+1} \tag{33}$$

The number of VM cells M and the turn ratios n and N affect the voltage stress across the VM diodes. The voltage stress across each of these diodes is equal, which can be given by (34):

$$V_{D_{VM1}}=V_{D_{VM2}}=\ldots=\frac{N+n(1-d)}{(1-\mathrm{d})^2}V_{in}=\frac{N+n(1-d)}{1+M\left(n(1-d)+N\right)}V_{out} \tag{34}$$

The average current that passes through switch S is expressed as (35):

$$I_S=dI_{Lm1}+dI_{Lm2}+\left(n+N\right)MI_{out} \tag{35}$$

The peak current when VM diodes D_{VM1}, D_{VM2}, … conduct can be obtained according to amp-sec balance law for the VM capacitors, which can be expressed as (36) and (37):

$$I_{D_{VM1}(peak)}=I_{D_{VM4}(peak)}=\ldots=\frac{2I_{out}}{d} \tag{36}$$

$$I_{D_{VM2}(peak)}=I_{D_{VM3}(peak)}=\ldots=\frac{2I_{out}}{(1-d)} \tag{37}$$

Furthermore, the peak currents that pass through diodes D_1 and D_2 can be expressed as (38):

$$I_{D1(peak)}=I_{D2(peak)}=I_{Lm1}+\frac{dV_{in}}{2L_mf_s}+\frac{nMI_{out}}{d} \tag{38}$$

E) Design of the Number of the Voltage Multiplier Cells and Turn Ratios

By considering the required optimum duty cycle and the desired output voltage for the proposed structure, the number of diode-capacitor voltage multiplier cells M, and the turn ratios n and N values can be determined. Based on (34), it can be concluded that the number of diode-capacitor voltage multiplier cells M affects the voltage stress on the voltage multiplier diodes. Thus, considering the peak inverse voltage of the chosen diodes (V_D^{Max}), the number of the employed diode-capacitor voltage multiplier cells M can be calculated as:

$$M\geq\frac{\left(n(1-d)+N\right)V_{out}-V_{D_{VM}}^{Max}}{\left(n(1-d)+N\right)V_{D_{VM}}^{Max}} \tag{39}$$

The turn ratios of the coupled inductors affect the voltage stress across the switches and voltage gain. Therefore, according to the drain-to-source break-down voltage of the chosen power switches $V_{(BR)DSS}$, the value of the turn ratio N is designed and can be expressed as follows:

$$n\geq\frac{V_{out}-V_{(BR)DSS}-NMV_{(BR)DSS}}{M(1-d)V_{(BR)DSS}} \tag{40}$$

The value of N can be obtained based on the desired voltage gain. Thus, according to the available input voltage V_{in}, the value of turn ratio N can be calculated as:

$$N=\frac{V_{out}-V_{in}-n(1-d)MV_{in}}{V_{in}} \tag{41}$$

F) Voltage Multiplier and Clamped Capacitors Design

In the presented topology, the voltage ripples across the capacitors should be within acceptable ranges to ensure an approximately constant output voltage. Therefore, designing the values of capacitors is essential. Thus, regarding the admissible voltage ripples across the capacitors, the values of capacitors can be computed.

Considering mode VII, the value of clamp capacitor C_{C1} can be calculated as (42):

$$C_{C1}\geq\frac{(1-d)n+N+d(2-d)}{(1-d)\Delta V_{Cc1}f_s}I_{out} \tag{42}$$

Also, considering mode III, the value of the second clamp capacitor C_{C2} is obtained as:

$$C_{C2}\geq\frac{dI_{out}}{\Delta V_{Cc2}f_s} \tag{43}$$

The values of voltage multiplier capacitors can be calculated as:

$$C_{VM1}=C_{VM4}=\ldots\geq\frac{I_{out}(1-d)}{\Delta V_{C_{VM}}f_s} \tag{44}$$

$$C_{VM2}=C_{VM3}=\ldots\geq\frac{I_{out}d}{\Delta V_{C_{VM}}f_s} \tag{45}$$

G) Efficiency and Loss Distribution

The RMS values of the component currents should be calculated to determine the mathematical efficiency of the presented topology. The equations of the RMS currents with their values (considering the characteristics presented in Table II) are tabulated in Table I. Also, the calculated loss breakdown of the laboratory prototype is presented in Table II. The equivalent series resistances of the coupled inductors' primary and secondary sides are denoted as r_{LP} and r_{LS}, respectively. Furthermore, in the proposed converter the core loss of each elected first and second cores at f_S=100 kHz are 1.3 W and 0.43 W, respectively. The power switches, power diodes, capacitors resistances, and the forward voltage of the power diodes are r_{DS}, r_D, r_C, and V_F, respectively.

IV. Closed-Loop Control System Design

In order to regulate the output voltage to a constant value a proper control method is required. To design a proper closed-loop control system, the converter's small-signal model is required. The state-space averaged model that is discussed in [29], is utilized to obtain the proposed converter's small-signal

model. In this structure, the currents of the magnetizing inductances (i_{Lm1} and i_{Lm2}) and the voltages of the clamp capacitors (V_{Cc1} and V_{Cc2}) are considered as the state variables. Thus, the small-signal model of the presented structure with M=1 can be defined as (46):

$$\dot{\tilde{x}} = A\tilde{x} + B\tilde{u} \quad ; \quad \tilde{y} = C\tilde{x} \tag{46}$$

where $\tilde{x}$, $\tilde{y}$ and $\tilde{u}$ are the state variables vector, output variables vector, and control signals vector, respectively. Regarding the method discussed in [29], the fixed matrixes $A_{n\times n}$, $B_{n\times r}$, and $C_{m\times n}$ can be obtained. It should be noted that n, m, and r are defined as the number of state variables, the number of output variables, and the number of control signals, respectively.

$$\tilde{x}^T = \begin{bmatrix} \tilde{i}_{Lm1} & \tilde{i}_{Lm2} & \tilde{v}_{Cc1} & \tilde{v}_{Cc2} \end{bmatrix}; \ \tilde{u} = [\tilde{d}]; \ \tilde{y} = [\tilde{v}_{out}] \tag{47}$$

The pole placement control method by the feedback of the integral state, which is shown in Fig. 4, can be a suitable control method for the proposed topology. In this control method, to locate the system's closed-loop poles to any appropriate areas via an appropriate design of the state-feedback gain matrix, the control system is required to be completely state controllable. From Fig. 4, (48) and (49) can be defined.

$$\tilde{u} = -K_x\tilde{x} - K_q q \tag{48}$$

$$\dot{q} = r - \tilde{y} = r - C\tilde{x} \tag{49}$$

In the above equations, r is the reference signals vector for the output variables and q is the integrator output. To investigate the complete state controllability of the system, the controllability matrix Φ_c, which can be defined as follows, should be obtained.

$$\Phi_c = \left[B' \middle| A'B' \middle| A'^2B' \middle| \ldots \middle| A'^{n-1}B' \right] = \left[B' \middle| A'B' \middle| A'^2B' \middle| A'^3B' \right] \tag{50}$$

The rank of the matrix Φ_c should be complete $rank(\Phi_c)=n=4$, to ensure that the system is completely state controllable.

Combining (46) and (49), the following matrixes can be obtained from the open-loop state matrixes:

$$\begin{bmatrix} \dot{\tilde{x}}(t) \\ \dot{q}(t) \end{bmatrix} = \underbrace{\begin{bmatrix} A' & 0 \\ -C' & 0 \end{bmatrix}}_{\tilde{A}'} \begin{bmatrix} \tilde{x}(t) \\ q(t) \end{bmatrix} + \underbrace{\begin{bmatrix} B' \\ 0 \end{bmatrix}}_{\tilde{B}'} \tilde{u}(t) + \begin{bmatrix} 0 \\ I \end{bmatrix} r(t); y(t) = \begin{bmatrix} C' & 0 \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ q(t) \end{bmatrix} \tag{51}$$

Also, the defined system in (51) should be completely state controllable. Therefore, if the rank of the matrix P is $m+n$, it can be concluded that the system is completely state controllable. The matrix P and its rank are defined as follows:

$$P = \begin{bmatrix} B' & A' \\ 0 & -C' \end{bmatrix}; \quad rank(P) = m + n = 5 \tag{52}$$

Equation (52) ensures the availability of a feedback matrix $K = [K_x \ K_q]$, which can locate the closed-loop poles in any desired areas. From Fig. 4, the state feedback matrix can be imported to the system of control as follows:

$$\tilde{u}(t) = -K\begin{bmatrix} \tilde{x}(t) \\ q(t) \end{bmatrix} = \begin{bmatrix} -K_x & -K_q \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ q(t) \end{bmatrix} \tag{53}$$

where K_q is integral gain constant and K_x is state feedback gain matrix.

Importing (53) into (51), the state space form of the closed-loop control system is obtained as follows:

$$\begin{bmatrix} \dot{\tilde{x}}(t) \\ \dot{q}(t) \end{bmatrix} = \begin{bmatrix} A'-B'K_x & -B'K_q \\ -C' & 0 \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ q(t) \end{bmatrix} + \begin{bmatrix} 0 \\ I \end{bmatrix} r(t); y(t) = \begin{bmatrix} C' & 0 \end{bmatrix} \begin{bmatrix} \tilde{x}(t) \\ q(t) \end{bmatrix} \tag{54}$$

By determining the appropriate closed-loop poles (eigenvalues) of (54), the value of the feedback matrix K can be obtained via the toolbox of the control system of MATLAB software. The designed control system will track the input reference $V_{out,ref}$ without any steady-state error because it has an integrator. The obtained bode-plots of the proposed system before and after implementing the pole-placement controller are illustrated in Fig. 5. To have a stable system, the gain margin of the system should be greater than 10, and the phase margin of the system should be obtained between 60° and 80°. Fig. 5 shows that the gain and phase margins of the converter system before implementing the controller are -57.6 and -40.2°, respectively. This means that the converter system is not stable before implementing the controller. After implementing the closed-loop pole-placement controller the gain and phase margins of the system are 10.7 and 69.3°, respectively. Therefore, the gain and phase margins of the closed-loop system have been optimized.

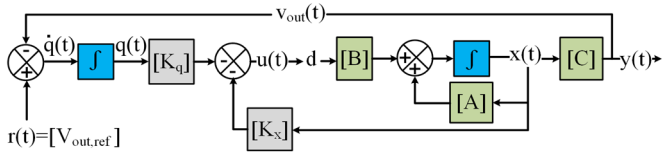


Fig. 4. Closed-loop control system schematic.

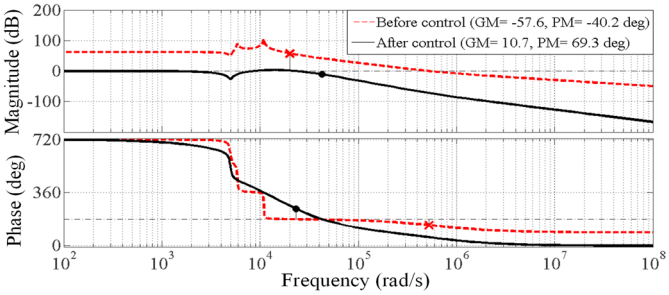


Fig. 5. Bode-plots for the transfer function of the output voltage

TABLE I
VARIOUS RMS VALUES OF THE CONDUCTING CURRENTS THROUGH THE COMPONENTS

$I^{RMS}_{L1,Secondary} = I^{RMS}_{L2,Secondary} = I_{out}/\sqrt{d(1-d)} = 2.5\ A$	$I^{RMS}_{C_{VM1}} = I_{out}\sqrt{(1-d)/d} = 1.25\ A$	$I^{RMS}_{L2,Primary} = \left(n(1-d)+N+d\right)I_{out}/(1-d) = 5\ A$
$I^{RMS}_{L1,Primary} = (1+(1-d)n+N)I_{out}/(1-d)^2 = 12.5\ A$	$I^{RMS}_{C_{VM2}} = I_{out}\sqrt{d/(1-d)} = 1.25\ A$	$I^{RMS}_{SAUX} = \left(n(1-d)+N+d\right)I_{out}/\sqrt{(1-d)} = 3.54\ A$
$I^{RMS}_{S} = \sqrt{d}\left((2-d)(1+N+n(1-d))+(1-d)^2\right)I_{out}/(1-d)^2 = 8.84\ A$		$I^{RMS}_{Cc2} = \sqrt{\left(\left[n(1-d)+N+2d-1\right]I_{out}/\sqrt{1-d}\right)^2 + dI^2_{out}} = 2.8\ A$
$I^{RMS}_{Cc1} = \sqrt{(1-d)\left(\left[d(2-d)+n(1-d)+N\right]/(1-d)^2\right)^2 + d\left(\left[N+n(1-d)+1\right]/(1-d)\right)^2}I_{out} = 9.1\ A$		$I^{RMS}_{D_{VM1}} = I_{out}/\sqrt{d} = 1.77\ A$
$I^{RMS}_{D_{VM2}} = I_{out}/\sqrt{1-d} = 1.77\ A$	$I^{RMS}_{D_1} = \sqrt{d}\,(3-d)I_{out}/(1-d)^2 = 8.84\ A$	$I^{RMS}_{D_2} = \sqrt{1-d}\,(3-d)I_{out}/(1-d)^2 = 8.84\ A$

TABLE II
LOSS DISTRIBUTION AND ANALYSIS OF EFFICIENCY

Type of power losses	Loss [W]	(Loss/Loss^{Total})
Core and conduction losses of the inductors	2.85	18.65 %
Conduction loss of S and S_{AUX}	0.73	4.78 %
Forward voltage loss of the diodes	8.1	53.01 %
Conduction loss of the diodes	1.69	11.06 %
Conduction loss of the capacitors	1.91	12.5 %
Total loss	15.28	Eff.%=97.03
V_{in}=40 **V**, P_{out}=500 **W**, V_{out}=400 **V**, N=n=1, f_S=100 **kHz**, d=0.5		
r_{LP1} =2.48 **mΩ**, r_{LS1} =6.5 **mΩ**, r_{LP1} =1.54 **mΩ**, r_{LS1} =3.3 **mΩ**		
S, S_{AUX}: IRFP4668PbF, r_{DS}= $r_{DS\text{-}AUX}$=8 **mΩ**		
D_1 and D_2: NTSV30H100CT, D_{VM1} and D_{VM2}: SBR20U150CT		
V_{F1}= V_{F2}= 0.52 **V**, r_{D1}=r_{D2}= 10 **mΩ**, $V_{F\text{-}VM1}$= $V_{F\text{-}VM2}$= 0.62 **V**		
r_{DVM1}=r_{DVM2}= 20 **mΩ**, r_{CVM1}=r_{CVM2}=30 **mΩ**, r_{Cc1}=r_{Cc2}=20 **mΩ**		

TABLE IV
THE EXPERIMENTAL PROTOTYPE SPECIFICATIONS

Parameter	Value
Duty cycle, output power	d=0.5, P_{out}=500 W
Input and output voltages	V_{in}= 40 V, V_{out}= 380 V
Switching frequency	f_S= 100 kHz
Power Switches S and S_{AUX}	IRFP4668PbF
Coupled inductors	L_{m1}= 70 µH, L_{m2}= 10 µH
Diodes D_1, D_2, D_{VM1}, and D_{VM2}	SBR10U300CT
Clamped capacitors	C_{C1}: 220 µF,160V; C_{C2}: 100 µF,160 V
Voltage multiplier capacitors	22µF, 160V
Snubber capacitor	C_S= 50 nF

V. PERFORMANCE COMPARISON

To determine the positives and negatives of the proposed structure, a comparison study, amongst the proposed structure and previously presented structures, is discussed in this section. The comparison results of the presented structure are summarized in Table III. Also, considering n = 2, the comparison results of the presented structure with the previous structures in terms of voltage gain and the voltage stress on the semiconductors are shown in Figs. 6 - 8. The comparison of the proposed converter with other topologies based on voltage gain versus various duty cycles is illustrated in Fig. 6. This figure demonstrates that the presented structure can provide the highest voltage gain with a minimum number of power switches and elements compared with structures with the same functions, especially the converters with ZVS performance. Table III shows that the number of elements in this structure is less than the number of elements in most of the other topologies (it is less than the number of elements in all of the soft-switching structures). Therefore, it is important to note that it is possible to obtain ultra-high voltage gains at optimum duty cycles.

The maximum normalized voltage stress across the main switch (V_S/V_{out}) versus the voltage gain is shown in Fig. 7. This figure indicates that the voltage stress across the power switches for a minimum number of elements (M=1) is lower than those from most of the other converters and the values are acceptable. Furthermore, the voltage stress across the switches declines significantly by raising the number of diode-capacitor voltage multipliers M.

Fig. 8 demonstrates the normalized maximum voltage stress on the diodes (V_D/V_{out}). Fig. 8 demonstrates that in the presented topology, the voltage stress on the diodes is within an admissible limited area. Moreover, the value reduces significantly by raising the number of diode-capacitor voltage multipliers M. Thus, by employing power switches with low voltage ratings in the presented topology, it is feasible to reduce the cost and conduction losses.

Fig. 9 shows the experimental efficiency comparison of the presented converter with the other reported converters. Fig. 9 shows that the proposed converter efficiency is the highest at 200 to 500 W output power ranges. Although the efficiency of the converter in [13] is a bit higher than the proposed converter efficiency at 100 to 200 W output powers, it is designed to work at these power ranges. Therefore, as it is obvious in the figure, its efficiency is going to be lower than the proposed converter efficiency at higher powers.

The comparison of the total voltage stresses across the utilized capacitors between the proposed converter and formerly presented structures is shown in Fig. 10. Fig. 10 shows that the total voltage stress across the capacitors of the proposed converter is minimum and equal to 1. Therefore, this allows the converter designer to use capacitors that can tolerate low voltage stresses. This feature reduces the size and cost of the converter.

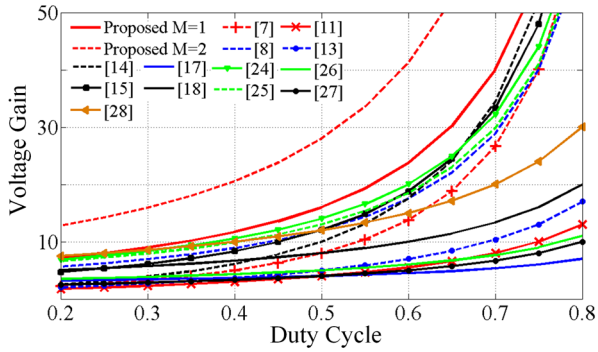


Fig. 6. Comparison of voltage gain versus various duty cycles.

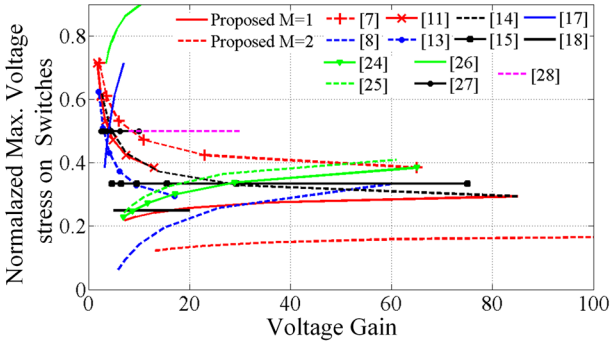


Fig. 7. Comparison of maximum voltage stress on switches versus voltage gain.

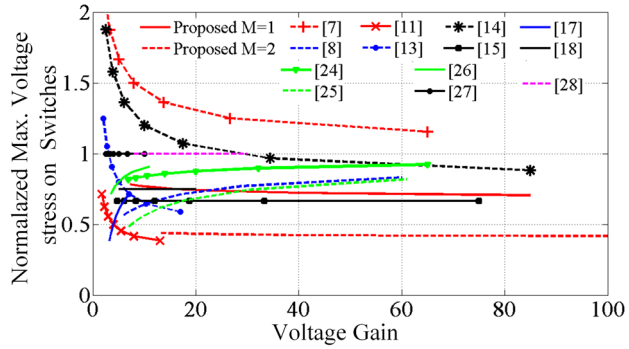


Fig. 8. Comparison of maximum voltage stress on diodes versus voltage gain.

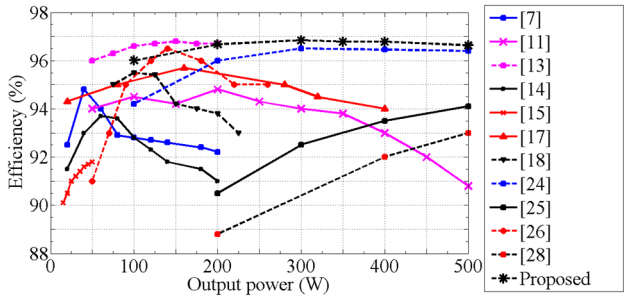


Fig. 9. Experimental efficiency comparison of the proposed converter.

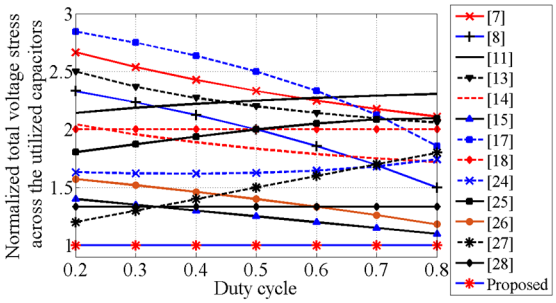
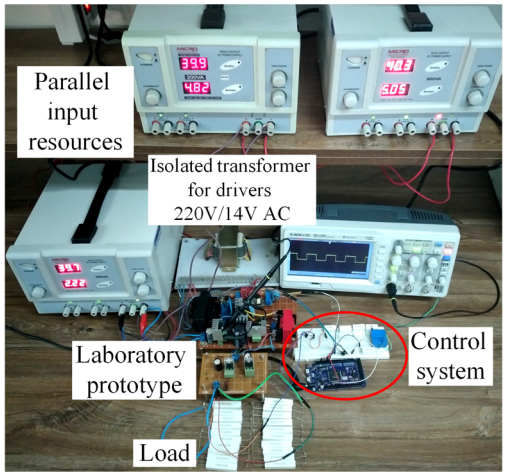


Fig. 10. Comparison of total voltage stress across the utilized capacitors with n=1.

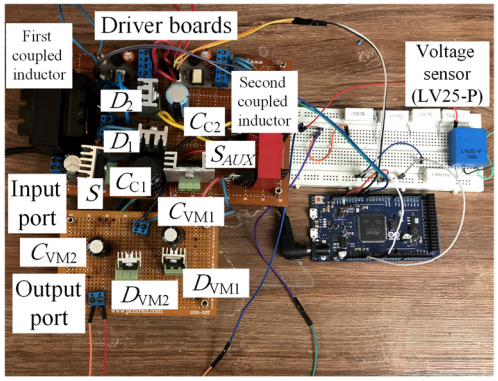
In addition to all of the mentioned merits, it can be added that in the presented topology, three degrees of freedom (n, N, and M) are provided for the designer to obtain the desired voltage gain and voltage stresses for the semiconductors with optimum duty cycle ranges. This amount of design flexibility has not been provided to the previously presented structures.

VI. Experimental Results

To validate the theoretical results, the experimental tests are carried out on a 500 W experimental prototype of the presented topology. The experimental setup and prototype photographs of the proposed converter are presented in Fig. 11. Table IV presents the specifications of the implemented laboratory prototype and Figs. 12-17 show the experimental results. Figs. 12(a) and 12(b) show the current through the leakage inductances L_{LK1} and L_{LK2}, and the waveforms of the input voltage and the capacitor C_{C2}.



(a)



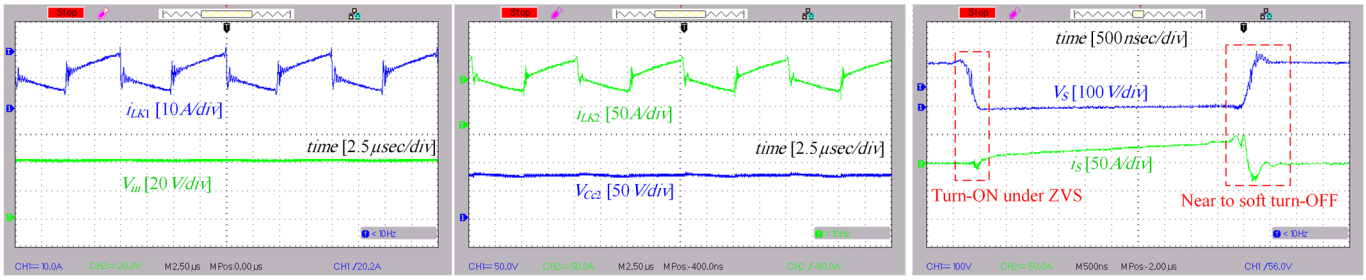
(b)

Fig. 11. Laboratory hardware test setup and prototype photographs of the proposed converter: a) hardware test setup, b) laboratory prototype.

TABLE III
COMPARISON OF THE PRESENTED CONVERTER WITH PREVIOUSLY PRESENTED STRUCTURES

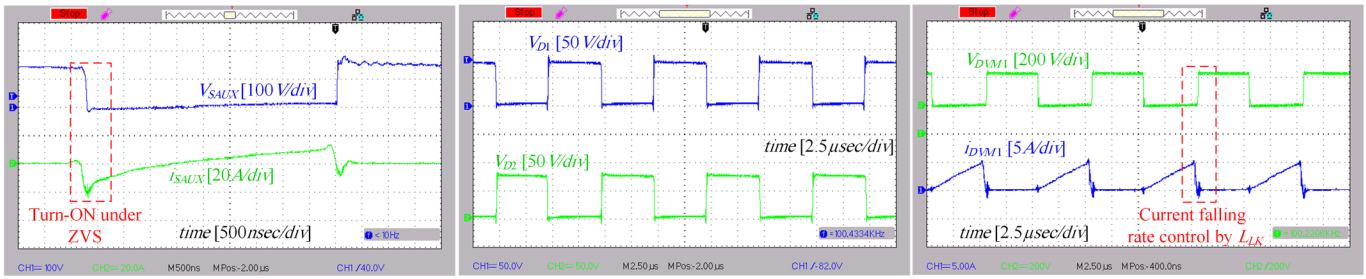
Ref.*	Voltage Gain	Normalized Maximum voltage Stress on switches	Normalized Maximum voltage Stress on diodes	Number of					Soft Switching of Switches
				*M. C.**	*S**	*D**	*C**	*T. D.**	
[7]	$(1+nd)/(1-d)^2$	$1/(1+nd)$	$(n+1)/(1+nd)$	3	1	6	4	14	-
[8]	$n(2-d)/(1-d)^2$	$d/n(2-d)$	$1/(2-d)$	2	2	5	4	13	-
[11]	$(1+2d)/(1-d)$	$1/(1+2d)$	$1/(1+2d)$	3	1	3	5	12	-
[13]	$(1+3d)/(1-d)$	$1/(1+3d)$	$2/(1+3d)$	3	2	2	3	10	-
[14]	$(1+d+nd)/(1-d)^2$	$1/(1+d+nd)$	$(1+n)/(1+d+nd)$	4	1	4	5	14	-
[15]	$(1+n)/(1-d)^2$	$1/(1+n)$	$n/(1+n)$	2	1	5	4	12	-
[17]	$((M+2)-(M+1)d)/(1-d)$	$1/((M+2)-(M+1)d)$	$1/((M+2)-(M+1)d)$	$1+M$	1	$3+M$	$3+2M$	$8+4M$	-
[18]	$(n+2)/(1-d)$	$1/(n+2)$	$(n+1)/(n+2)$	2	1	3	4	10	-
[24]	$(1-d+n(2-d))/(1-d)^2$	$1/(1-d+n(2-d))$	$n(2-d)/(1-d+n(2-d))$	2	3	3	4	12	ZVS
[25]	$[(1-d)^2+n(2-d)]/(1-d)^2$	$1/[(1-d)^2+n(2-d)]$	$n/[(1-d)^2+n(2-d)]$	2	4	4	5	15	ZVS
[26]	$(3-d)/(1-d)$	$2/(3-d)$	$2/(3-d)$	3	2	5	3	13	ZVS
[27]	$n/(1-d)$	$1/n$	1	4	4	4	2	14	ZVS
[28]	$3n/(1-d)$	$1/n$	1	4	4	6	2	16	ZVS
Prop.*	$(M(2-d)n+1)/(1-d)^2$	$1/(M(2-d)n+1)$	$M(2-d)n/(M(2-d)n+1)$	2	2	$2+2M$	$2+2M$	$8+4M$	ZVS

C^*: Capacitor; D^*: Diode; Prop.*: Proposed converter; *M. C.**: Magnetic core; Ref.*: Reference; S^*: Switch; *T.D.**: Total device.



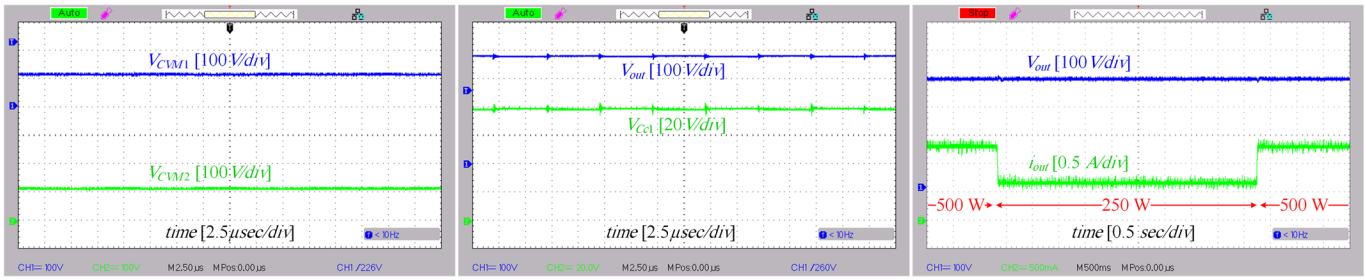
(a) (b) (c)

Fig. 12. Experimental results at 0.5 kW output power: a) input voltage V_{in} and the conducting current through leakage inductance L_{LK1}, b) voltage across the clamped capacitor C_{C2} and the conducting current through leakage inductance L_{LK2}, and c) voltage and current of the main switch S.



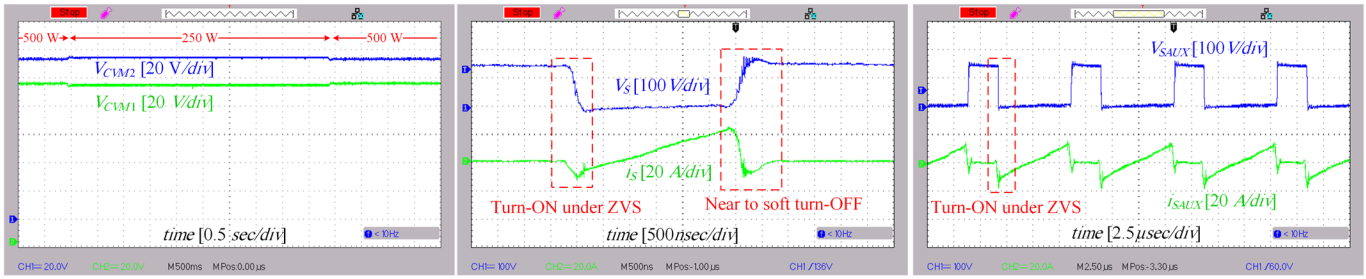
(a) (b) (c)

Fig. 13. Experimental results at 0.5 kW output power: a) voltage and current of the auxiliary switch S_{AUX}, b) voltages across the diodes D_1 and D_2, and c) voltage and current of voltage multiplier diode D_{VM1}.



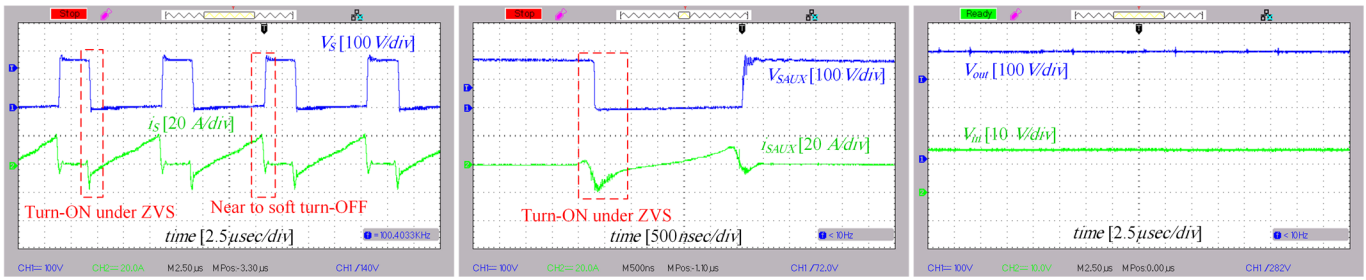
(a) (b) (c)

Fig. 14. Experimental results: a) voltages across voltage multiplier capacitors C_{VM1} and C_{VM1} at 0.5 kW output power, b) voltage of capacitor C_{C1} and output voltage V_{out} at 0.5 kW output power, and c) dynamic response of the output voltage during load transients.



(a) (b) (c)

Fig. 15. Experimental results: a) dynamic response of the voltages across the voltage multiplier capacitors during load transients, b) voltage and current of the main switch S at 250 W output power, and c) voltage and current of the auxiliary switch S_{AUX} at 250 W output power.



(a) (b) (c)

Fig. 16. Experimental results: a) voltage and current of the main switch S at 50 W output power, b) current and voltage of the auxiliary switch S_{AUX} at 50 W output power, and c) input and output voltages with duty cycle 0.7.

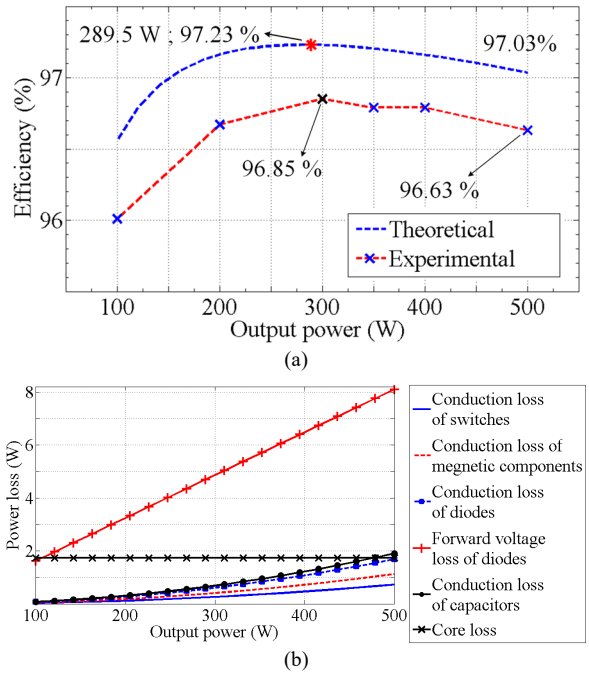


Fig. 17. Efficiency and loss distribution of the presented converter at 100 W to 500 W output powers: a) experimental and theoretical efficiency and b) loss distribution.

Fig. 12 demonstrates that the input current average value (or I_{LK1}) is 13 A with 12.5 A ripple for 40 V input voltage, which confirms the theoretical calculations. Also, the voltage across the clamped capacitor C_{C2} is measured to be 77 V, which confirms (18). Fig. 12(c) illustrates the voltage and current waveforms of the main switch *S*. Fig. 12(c) shows that switch *S* turns on under zero voltage switching performance. Also, the snubber capacitor of switch *S* leads the switch to turn off with low overlapping voltage and current. Fig. 13(a) demonstrates not only the voltage and current waveforms of the auxiliary switch but also the operation of the switch under the ZVS condition.

Fig. 13(b) shows the voltage waveforms across diodes D_1 and D_2. The voltages across the diodes are measured to be 78 V, which validate (31) and (32). The current and voltage waveforms of the voltage multiplier diode D_{VM1} is indicated in Fig. 13(c). This figure demonstrates that the rate of the current drop of the VM diodes is controlled by the coupled inductors leakage inductances L_{LK1} and L_{LK2}. Thus, the reverse recovery losses of the VM diodes are significantly decreased.

The experimental voltage waveforms of VM capacitors C_{VM1} and C_{VM2} are shown in Fig. 14(a). The VM capacitors voltages are calculated to be 120 V from (19) and (20) and measured to be 113 V. Thus, the experimental results confirm the mathematical calculations. Fig. 14(b) illustrates the voltage across the clamp capacitor C_{C1} and output voltage for 40 V input voltage. The calculated output voltage V_{out} and V_{Cc1} are 400 V and 80 V (from (22) and (17)), which are near to their measured values of 380 V and 78 V, respectively.

Fig. 14(c) shows the dynamic response of the output voltage of the proposed converter during load transients from full load to half load and vice versa. This figure demonstrates that the output voltage can be regulated immediately to the constant value of 380 V with a small voltage variation during the step load change. Fig. 15(a) shows the voltage balances of the VM capacitors during the load transients. Fig. 15(a) shows that the voltage across the capacitor C_{VM1} increases, the voltage across the capacitor C_{VM2} decreases, and vice versa, which confirms (19) and (20).

Figs. 15(b) and 15(c) show the current and voltage waveforms of both the switches at half load condition, with duty cycle 0.3. As it is clear in the figures, the ZVS turn-on for both the switches is realized at duty cycle 0.3 and the half-load condition. Also, the main power switch turns off at this condition with near to soft-switching condition. Figs. 16(a) and 16(b) illustrates the current and voltage waveforms of both the switches at 50 W output power and 0.7 duty cycle. Both the switches *S* and S_{AUX} turn on under ZVS condition at 0.1 full-load and duty cycle 0.7. As well, the main power switch turns off with near to soft-switching condition. Therefore, it can be concluded that by doing a proper design ZVS can be obtained at all power and working duty cycle ranges.

Fig. 16(c) shows the input and output voltages' experimental waveforms with duty cycle 0.7. Fig. 16(c) shows that the proposed converter can reach the voltage gain of 24.4 easily just by increasing the duty cycle value without increasing the turn ratios and adding VM stages.

Fig. 17(a) illustrates the obtained theoretical and experimental efficiencies of the presented topology at 100 W to 500 W output powers. The maximum theoretical efficiency of the converter is 97.23% at 289.5 W output power, where it is found to be 96.85% at 300 W output power. Also, at 500 W output power, the experimental efficiency is measured to be 96.63%, where the theoretical value is 97.03%. Therefore, the experimental efficiency is close to the theoretical efficiency which confirms the theoretical results. Moreover, the theoretical loss proportion of components at 100 to 500 W output powers is shown in Fig. 17(b), which demonstrates that the major loss component is the forward voltage loss of diodes. This loss value increases as the output power increase. Also, the core losses can be considered as major losses, however, this value is relatively constant, and its effect reduces as the output power increases.

VII. CONCLUSION

This paper presents a new ultra-high voltage gain dc-dc boost converter with ZVS capability. The detailed analysis of the various operational modes and the design of the diverse components of the proposed topology are discussed. In the presented topology, the technique of using coupled inductors and extendable diode-capacitor VM cells is employed to raise the voltage gain. Also, three degrees of freedom are supplied via the number of voltage multiplier stages and the coupled inductors turn ratios. These degrees of freedom provide flexibility to the designer to set the desired voltage stresses on the diodes and switches within the desired range. Also, the proposed topology has the feature to be designed flexibly to provide a high voltage gain at optimum duty cycles. Although the presented topology has two coupled inductors, the second coupled inductor value should have a low value. This will help to reduce the converter volume and cost. Moreover, in the proposed topology, both the switches operate under zero voltage switching. Also, the rate of the current drop of the VM diodes is controlled by the coupled inductors leakage

inductances. Finally, to validate the characteristics and theoretical analysis, laboratory experiments are carried out using a 40 to 380 V and 500 W laboratory prototype. The experimental results are shown to be close to the theoretical calculation.

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